


Surround Sound Retrieval System

By:
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Mr. Joe Kulathinal
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Dear Mr. Kulathinal:

Please find inclosed a copy of my technical report on the Surround Sound Retrieval System. The analysis and design of this technical report has successfully operated in the goal set out for.

In being an electronics student at DeVry, I have gained a great understanding in analog control circuitry and knowledge in electronics in general. During the past year at DeVry, I have learned so much from your classes. This to me is essential in understanding how things are related in the industry.

I would like to take the time and thank you for your time and great assistance in the completion of this technical report. I have learned so much. Thanks again.

Yours very Truly,

Randy Allensen

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ABSTRACT

The main objective of this technical report is to create **"surround sound"**. It is the **"realization"** of being there. This objective is accomplished by processing the input signals and reconstructing the processed signals at the output. Hence **surround sound** is created.

INTRODUCTION

This technical report is based on the Dolby-stereo surround sound audio system developed by Dolby laboratories in the 1970's. This surround sound creates the "realization" of being there. It creates distinct sounds to the front, rear and sides of the viewer or listener. This Dolby surround sound process can be recreated with relatively simple circuit elements. The basic principle of surround sound decoders is to reproduce the surround information by recovering the (L - R) difference signal which is encoded into the left and right channels of a movie soundtrack.

Extra circuitry is used in addition to the (L - R) circuitry to create wide left, wide right, centre dialogue and subwoofer signals. Introducing these signals to six properly arranged speakers results in the acoustical illusion of a large, three dimensional listening environment.

The first accountable point that is taken into consideration when dealing with audio systems, is the way the human ear perceives sounds. Humans perceive sounds that come about from at least three different means. Detection of relative phase of sounds in the case of the lower frequencies is between 20 Hertz and 200 Hertz. For mid-range sounds, they are accountable between 300 Hertz and 4000 Hertz and with this extent of mid-range frequencies, we detect the relative intensity. Generally speaking sounds coming from one side sound louder to the nearest ear and softer to the other ear.

For the high frequencies, those that have a fast rise time; we judge direction by the relative time of arrival. These sounds reach the closest ear sooner than they reach the farther one. A fourth factor governs in which we perceive sounds (where sounds originate). This factor is the way our hearing system's frequency response varies (see figure 1-page #6).

The pinna (known as the outer ear) has an effect on the spectrum of the sound reaching the eardrum. The concha (the section that leads to the ear canal) has an effect on the frequency at which the ear canal is resonant. Working together, these two parts of the ear control the spectral shape (frequency response) of the sounds reaching the eardrum. Therefore the ear can basically be described as

sort of a multiple filter, emphasizing some frequencies, attenuating others or letting some through unaffected. The ear's frequency response changes to both distance and elevation. When these two factors are put together with our binaural (two ear) capabilities, they help us determine sounds coming from above, below, the left, the right, ahead or behind. Examples on how our hearing systems respond to frontal sounds, sounds from the sides and from behind are shown in figure 2-page #7. Figure 3-page #8 shows the ambient, reflected and side signals producing a complex sound field.

Another accountable point that has to be taken into consideration when dealing with audio systems is how the brain interprets various sounds that the ear's perceive. The brain integrates two sounds and perceives them as a single sound when the ears perceive these sounds that are identical in form (waveshape and amplitude) and are time displaced by less than 10 milliseconds. The brain perceives two sounds as two independent sounds, but integrates their information content into a single easily recognizable pattern with no loss of information fidelity (accuracy of reproduction) if the ears perceive the two sounds that are identical in form but time displaced by 10 to 50 milliseconds.

If two sounds are identical in shape but not in magnitude and are time-displaced by more than 10 milliseconds, the ears perceive these two sounds and the brain interprets them as two sound sources (primary and secondary). The brain draws conclusions on the distances between the two sources and the location of the primary source. The brain interprets the first perceived signal as the primary sound source. This fact is regarding to the location definition. Even if the first perceived signal is lower in relative amplitude than that of the second perceived signal, the brain still interprets the first perceived signal as the primary sound source. This is known as the Hass effect. For the identification of distance, the brain correlates distance and time-delay at roughly 0.3 meters (about 13 inches) per one millisecond of delay. Therefore a delay line can be used to trick the brain in telling about how far apart two sound sources really are. Now that how the ears perceives sounds and how the brain interprets these sounds has been explained, the processing of the input signals can now be described in the signal processing section.

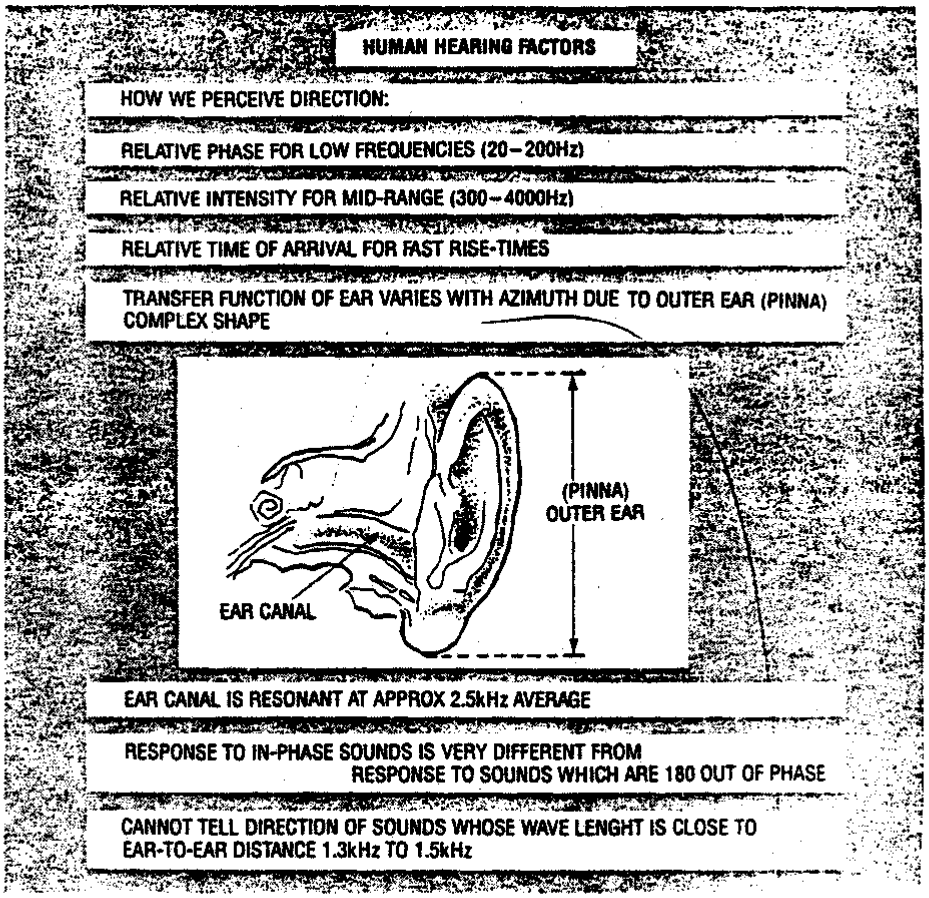


Figure 1. The Fourth Factor: the way in which we judge where sounds originate.

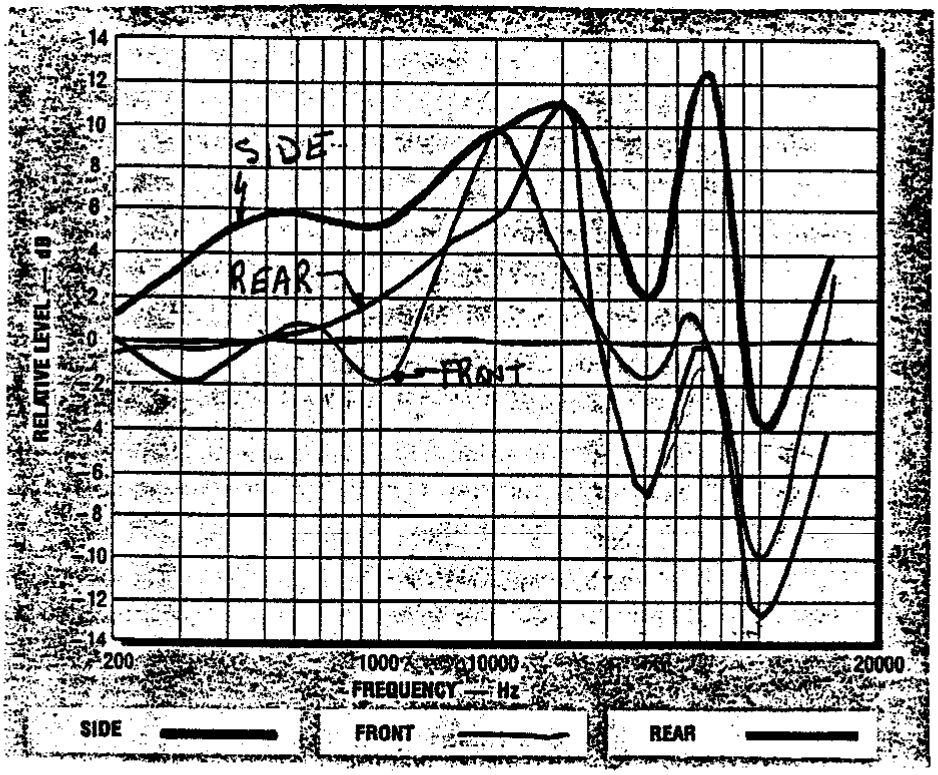


Figure 2. The EAR's Frequency Response. Our hearing system's response to frontal, side and rear sounds.

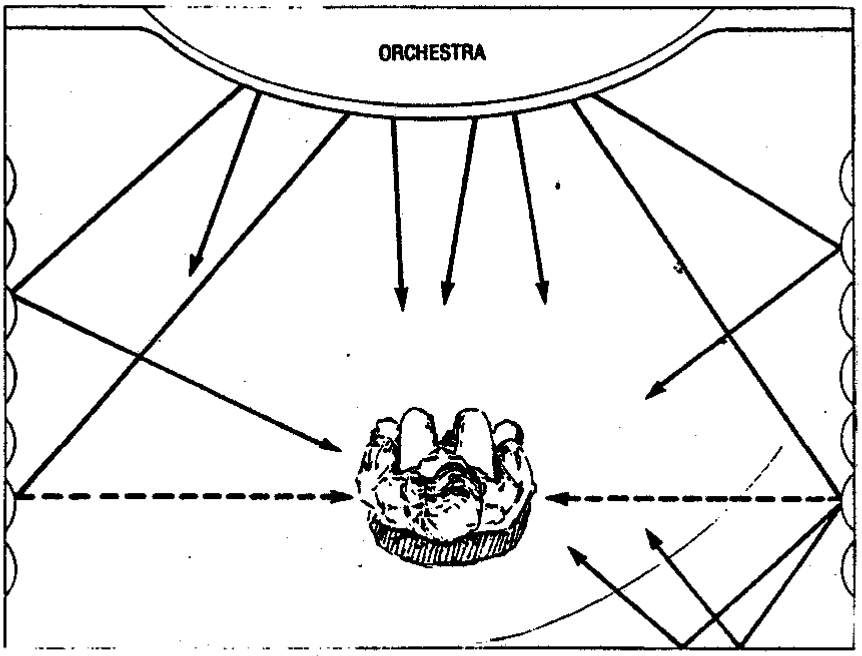


Figure 3. Ambient, Reflected and Side Signals produce a complex sound field.

SIGNAL PROCESSING CIRCUIT

THEORY:

The input LEFT and RIGHT signals must be processed first in order to create **surround sound** (a three dimensional listening environment). This processing of the LEFT and RIGHT signals is accomplished by the processing circuit (circuit # 1) and can be found in appendix A. Surround sound is accomplished by taking two input signals (left and right) and processing them into other signals. A (L - R) difference signal, a (L + R) summation signal, two wide signals and a subwoofer signal. The (L - R) and (L + R) signals are delayed. A switch (S1) can control which of these signals are to be delayed. This delayed signal will appear in a pair of speakers located to the rear of the listener. The (L + R) summation signal is fed into a centre channel bandpass filter. The output signal of this filter drives a pair of centre speakers located to the centre of the listener. The original signals are processed into yet another pair of signals; **LEFT WIDE** and **RIGHT WIDE** signals. These pair of signals drive a pair of speakers located to the front of the listener.

Note: All circuit diagrams (circuits 1 through 5) are illustrated in Appendix A.

The signal processing circuit contains the following circuit elements:

1. Two unity gain buffer amplifiers.
2. A variable gain differential amplifier.
3. A Non-inverting summing amplifier.
4. Two WIDE signal production circuits.

1. UNITY GAIN BUFFER AMPLIFIER

Theory:

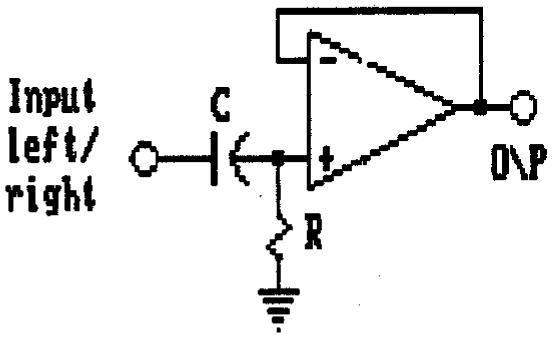


Figure 1. Unity Gain Buffer Amplifier.

Only one unity gain buffer amplifier is shown because the other buffer amplifier is exactly the same. Both right and left signals are buffered at the input of the signal processing circuit (circuit # 1). The reason for this is to prevent the other parts of the circuit from being loaded down when the input frequency of both channels vary. The input of the buffers are from either the left or right channels. The buffers transform the 47.5 kilohm input

impedance to a low impedance source which drives all of the amplifiers, filters and by-pass outputs. The resistor capacitor combination produces a cutoff frequency of approximately 1.5 Hz. All frequencies above this cutoff will be passed. Which is suitable because the audio range is from 20 Hz to 20000 Hz.

Design:

The transfer function of the unity gain buffer amplifier is as follows:

$A(s) = R/(R + 1/sC) = RCs/(RCs + 1)$

dividing by RC

$= s/(s + 1/RC)$

The transfer function is in high-pass form, where:

$Wc = 1/RC \implies 1$ Wc was assumed to be 10 r/s and C = 2.2 μf, R was calculated using equation 1.

$R = 1/(Wc*C) = 1/(10*(2.2*10^{-6})) = 45455.55\ \Omega$

Components Used For Figure # 1 are as Follows:

R = 47.5 kΩ

C = 2.2 μf

2. VARIABLE GAIN DIFFERENTIAL AMPLIFIER

Theory:

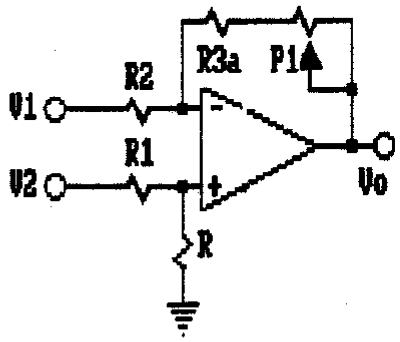


Figure 2. Variable gain Differential Amplifier.

In order for the differential amplifier to work properly, it is required to match R2=R1, R3=R (R3 being the combination of R3a and P1). Therefore the differential amplifier is a combination of an inverting and non-inverting amplifiers. When V1 is reduced to zero the circuit is a non-inverting amplifier, whereas the circuit is an inverting amplifier when the input V2 is reduced to zero. The differential amplifier also presents a balanced input impedance. Ideally a differential amplifier must totally ignore the common mode signal and amplify the difference signal => Quality Factor: CMRR Common Mode Rejection Ratio (20 log (A_d/A_c). One input => the other input is called the differential input (V_{id}). Common-mode input => a signal common to both inputs (V_{inc}).

The (L - R) difference signal is accomplished by this variable gain differential amplifier. The differential

amplifier has two inputs. One from the output of the left channel buffer and the other from the right channel buffer. Having a pot (P1) in series with a 47.5 kilohm resistor across the negative feedback varies the amount of common mode signal that will appear at the output of the differential amplifier. The resistor in series with the pot is required because R3 is supposed to equal R. If the resistor was not in series with the pot and the pot adjusted to zero ohms, the output would go to into saturation, which is not the practical use of this circuit (figure # 2).

When the pot (P1) is adjusted right to zero, the common-mode signal is fully rejected meaning the signals common to both the left channel and right channel are rejected. Since the signals common to both channels are rejected, it forms one signal which contains none of the common **"mono"** information present in the original stereo signal. Therefore, only signals different form each other are allowed to pass to the output, which is the (L - R) difference signal. If the pot (P1) is gradually adjusted higher, some of the common mode signal is passed through to the output. The more this pot (P1) is adjusted higher, more of the common mode signal is passed. The varying of this pot (P1) is called **"MONO NULL"**. It is called this because by adjusting P1, the signal common to both channels will be rejected, or by gradually adjusting the pot the other way, some of the common mode signal are passed as well as with

signals different from each other as mentioned previously. When the pot is adjusted gradually to its maximum value of 100 kilohms, the gain increases (to times 3). The overall effect of the output of this circuit (figure # 2) is controlled by the pot (P1) giving an output of the operational amplifier of difference signal only. This difference signal is then applied to the delay circuit (circuit # 2), which will be described later. S1 of the signal processing circuit (circuit # 1) determines which signal is to be delayed; the difference signal (L - R) or the summation signal (L + R).

Design:

To check the practical operation of the differential amplifier, equations 1, 2 and 3 can be used.

$$V_{o1} = -(R3/R2)*V_1 \quad ====> \quad 1$$

$$V_{o2} = (R3/R2 + 1)*(R/(R + R1)*V_2 = (R3/R2)*V_2 \quad ====> \quad 2$$

$$V_o = V_{o1} + V_{o2}$$

$$= -(R3/R2)*V_1 + (R3/R2)*V_2$$

$$= (R3/R2)*(V_1 - V_2) = [R3*(V_{12})]/R2$$

$$A_d = V_o/V_{12} = -R3/R2 \quad ====> \quad 3$$

For the determination of the circuit components of figure # 2, it was required to match R3 = R (where R3 is the combination of R3a and P1) and match R2 = R1. P1, R3a, R2, R1 and R were arbitrarily selected (keeping in mind the matching conditions).

Components Used For Figure # 2 are as Follows:

P1 = 100 kΩ

R = R1 = R2 = R3a = 47.5 kΩ

3. NON-INVERTING SUMMING AMPLIFIER

Theory:

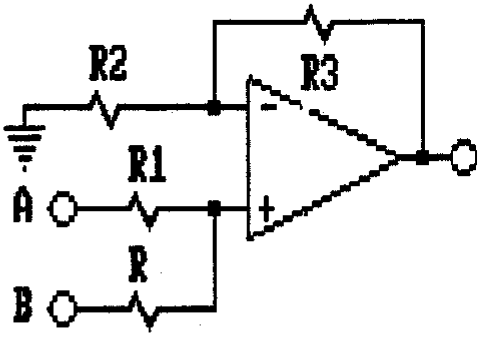


Figure 3. Non-inverting Summing Amplifier.

The (L + R) summation signal is accomplished by a non-inverting summing amplifier. Both output signals from the buffers (left and right) are summed together combining equal amounts of the left and right signals to develop a total composite signal. The input A of this amplifier is connected to the output of the right channel buffer and input B of the amplifier is connected to the output of the left channel buffer as shown in circuit # 1-appendix A. The amplitude of the output signal (L+R) is controlled by the feedback resistor (R3). If one of the input resistors were changed, the output would change accordingly because the one input signal would be higher in amplitude than that of the other. Equation number one was used for the design of the non-inverting summing amplifier (figure # 3) with a gain of 1.619.

Design:

$V_{o1} = [R/(R + R1)]*[((R3/R2) + 1)]*V_1$

$V_{o2} = [R1/(R + R1)]*[((R3/R2) + 1)]*V_2$

$V_o = V_{o1} + V_{o2}$

$= [R/(R + R1)]*[((R3/R2) + 1)]*V_1 + [R1/(R + R1)]*[((R3/R2) + 1)]*V_2$

$= [((R3 + R2)/R2)]*[((R + R1)/(R + R1))*(V_1 + V_2)]$

$V_o = ((R3/R2 + 1))*(V_1 + V_2)$

$V_o/(V_1 + V_2) = (R3/R2) + 1 \quad ====> \quad 1$

The gain of 1.619 and R3 was arbitrarily selected. A(v) = 1.619 and R3 = 61.9 kΩ, R2 was calculated using equation # 1.

$V_o/(V_1 + V_2) = (R3/R2) + 1$

$1.619 = (61.9 * 10^3/R2) + 1$

$-(61.9 * 10^3/R2) = 1 - 1.619$

$R2 = 61.9 * 10^3/0.619 = 100$ kΩ

R1 and R were required to be equal. This condition is needed to get equal amounts of left and right signals to be summed together.

Components Used For Figure # 3 are as follows:

R3 = 61.9 kΩ

R = R1 = R2 = 100 kΩ

4. WIDE Signal Production Circuit

Theory:

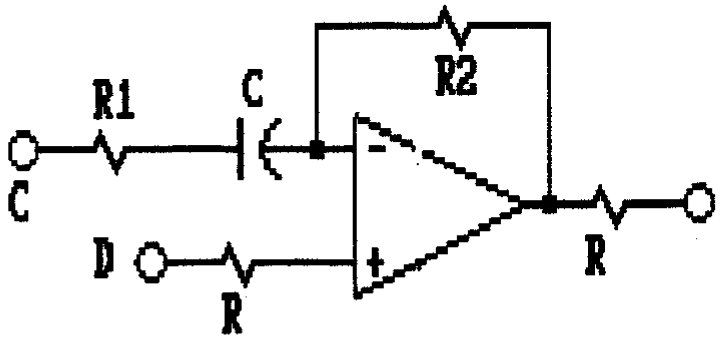


Figure 4. A WIDE signal production Circuit.

The stereo width enhancements is made up from a WIDE production circuit (figure # 4). Consider the right wide production circuit (IC2-d) of the signal processing circuit (circuit # 1). C and R1 form a gently sloping high-pass filter response for the left channel signal only. The amount of signal cancellation is dependent on frequency and the relative amplitude between the two channels. Therefore the more the signal is the same in both channels, the more it is removed from the output of the circuit. This effect increases as the signal's frequency rises. If the signal appears in the right channel only (point D), no matter what its frequency or amplitude, it appears at the output unaffected. The LEFT WIDE signal is accomplished the same way, except its inverting (point C) and non-inverting (point D) inputs are connected to the left and right channels in a way opposite of the RIGHT WIDE production circuit. The

final effect of the WIDE signals is to increase the apparent separation between left and right channels by eliminating some of the material common between them. The LEFT WIDE and RIGHT WIDE signals produced by figure # 4 are routed to S3-c and S3-d. These switches determine which signals feed the front channel amplifier. The normal unaffected left and right signals or the LEFT WIDE and RIGHT WIDE signals.

Design:

Consider a moment that point D in figure # 4 is grounded. Point D in the circuit is grounded because R2, R1 and C can then be solved for. The circuit (figure # 4) now becomes an inverting high pass filter with R1 and C determining the cutoff frequency and R2, R1 controlling the gain of the filter.

The transfer function of this high-pass filter configuration is as follows:

$$A_{(s)} = R2/(R1 + 1/sC) = R2Cs/(1 + R1Cs)$$

dividing by R1C

$$= (R2/R1)*s/(s + 1/R1C)$$

The transfer function is in high-pass form, where:

$A_v = -R2/R1$ ====> 1

$W_c = 1/R1C$ ====> 2

W_c was assumed to be 213 rads/sec and $A_v = -1$.

R1 was arbitrarily selected to be 100 kΩ. Using equation # 1, R2 was calculated.

$$A_v = -R2/R1$$

$$-1 = -R2/100 * 10^3$$

$$R2 = 100\ k\Omega$$

Using equation # 2, C was calculated.

$$W_c = 1/R1C$$

$$213 = 1/(100*10^3*C)$$

$$C = 1/(100*10^3*213) = 0.046948\ \mu f$$

Now disconnecting point D from ground yields the circuit of figure # 4. The actual output voltage can be found of the circuit (figure # 4). This output voltage is as follows:

First grounding point D, V_{o1} is as follows:

$$V_{o1} = -R2/(R1 + 1/sC)*C = [-R2Cs/(1 + R1Cs)]*C$$

Note: Point C is the first input voltage of figure # 4. Then grounding point C, V_{o2} becomes:

$$V_{o2} = [R2/(R1 + 1/sC) + 1]*D = [R2Cs/(1 + R1Cs) + 1]*D$$

Note: Point D is the second input voltage of figure # 4.

$$V_o = V_{o1} + V_{o2}$$

$$= [-R2Cs/(1 + R1Cs)]*C + [R2Cs/(1 + R1Cs) + 1]*D$$

$$V_o = (1/R1Cs) * [-(R2Cs)*C + ((R1 + R2)Cs + 1)*D]$$

R is arbitrarily selected to be 100 kΩ, even though it doesn't really do anything in the circuit (figure # 4).

<u>Components Used For Figure # 4 are as follows</u>:

R = R1 = R2 = 100 kΩ

C = 0.047 μf

DELAY CIRCUIT

Theory:

In analyzing the delay circuit some delay-line basics should be known. The CTD (Charge Transfer Device) or bucket-brigade delay line is the integrated circuit form of modern analog delay lines. These devices contain a number of analog memory cells (buckets). A cell is actually a sample-and-hold circuit. Usually the device has 512, 1024, 4096 cells wired in series. In this case with the MN3007 of the delay circuit (circuit # 2-appendix A), it is 1024 cells. Meaning this chip has 1024 stages. Analog signals are applied to the input of the first cell and the delayed output is taken from the last cell.

Each bucket (cell) consists of a small valued capacitor and a MOSFET which function together as a sample-and-hold stage. The input signal of the BBD (bucket brigade device) will appear at the output at a later time as compared to the original input signal. This time depends on both the clock frequency applied to the BBD (supplied by the 2-phase clock frequency generator-MN3101) and the number of stages of the BBD. Now that some delay line basics are known, the analysis of the signal will now be explained as it travels through the delay circuit (circuit # 2).

The delay circuit is built around the MN3007 Bucket Brigade Device (BBD) and the MN3101 variable two-phase clock frequency generator, both made by Matsushita (Panasonic). The BBD is a P-channel silicon-gate MOS LSI circuit made up of 1024 bucket brigade stages fabricated on a single chip. Each stage of the BBD consists of a small capacitor that stores an electric charge and a tetrode transistor (as mentioned previously) for switching purposes. When an analog signal is applied to the BBD, an electrical charge corresponding to the input analog signal is transferred from one stage to the other by a two-phase clock frequency drive. This can be related to a fireman's bucket brigade that transfers a pail of water from on man to the next.

The input signal of the delay line is applied to a third-order low-pass filter. Cascading two identical third-order 15 kHz low-pass filters, produces a very sharp cutoff of -36 dB per octave (which is -60 dB per decade), which is convenient as it eliminates any problems with aliasing. At the same time maintaining a respectable 15 kHz bandwidth. Aliasing meaning if the incoming frequency is more than one-half the slowest clock frequency, ± frequencies above and below half the clock frequency may be produced. So a filter placed before the BBD is essential if it is desired to run the clock at its minimum frequency (maximum delay). The input signal is then applied to the input of the BBD. This signal is transferred down each stage at a speed controlled

by the frequency of the clock. Therefore the amount of delay at the output of the BBD is the number of stages divided by two times the clock frequency. The delayed signals of the BBD are reconstructed at the output. The design of this delay circuit is now explained keeping in mind aliasing. The delay circuit (circuit # 2) contains the following circuit elements:

1. A Variable Gain Inverting Amplifier.
2. Three Third-order 15 kHz Low-pass Filters.
3. A Two-phase Clock Frequency Generator (MN3101).
4. A Bucket Brigade Device (BBD-MN3007).

1. VARIABLE GAIN INVERTING AMPLIFIER

Theory:

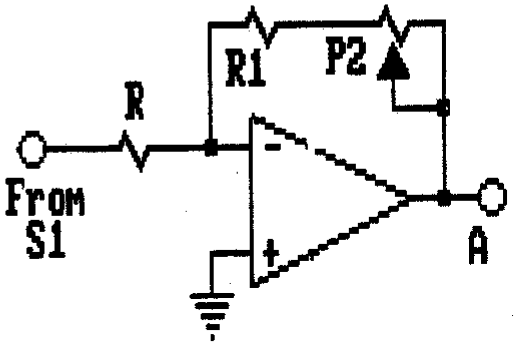


Figure 1. A Variable Gain Inverting Amplifier.

The incoming signal from S1 is inverted. This incoming signal can be either (L - R) or (L + R). This inverting amplifier (figure # 1) varies from unity gain to a gain of

times 3. The purpose of this inverting amplifier is to control the amplitude of the incoming processed signal to the rest of the delay circuit. After the incoming processed signal is inverted, it gets directed to just one of the 15 kHz low-pass filters that exist before the BBD.

Design:

The following design equation was used in the design of the variable gain inverting amplifier.

$A_v = -Rf/Ri \implies 1$, where $Rf = P2 + R1$ and $Ri = R$

The overall gain was chosen: $A_v = -3$

P2 and R1 were assumed to be:

P2 = 100 kΩ, R1 = 47.5 kΩ, R was calculated using equation # 1.

$-3 = -147.5*10^3/Ri$, $R = Ri = -147.5*10^3/-3 = 49.16$ kΩ

The Components Used For Figure # 1 are as Follows:

P2 = 100 kΩ

R = R1 = 47.5 kΩ

2. THIRD-ORDER 15 KHz LOW-PASS FILTER

Theory:

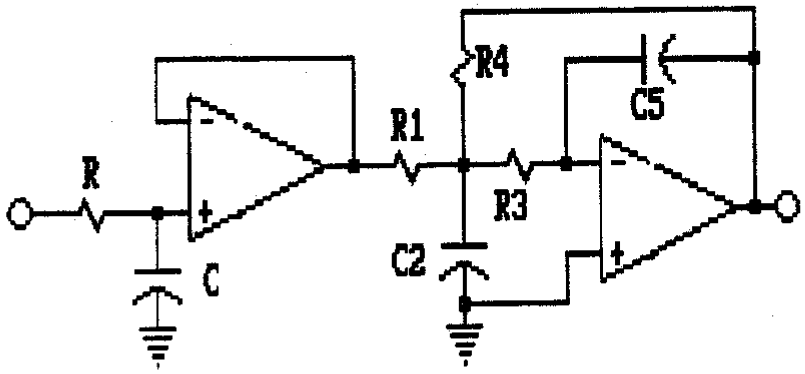


Figure 2. Third-Order 15 kHz Low-pass Filter.

In the overall delay section, three third-order 15 kHz low-pass filters are used. Only one filter is shown because the other two are exactly the same. The third-order 15 kHz low-pass filter (figure # 2) has two stages. The first stage is of a first-order non-inverting low-pass filter. The second stage is of a second-order inverting low-pass filter. When both stages are put together, it forms a third-order low-pass filter. In designing a third-order low-pass filter, it is a requirement to make both stages cut off at the same frequency. In other words the frequency scaling factor is required to be the same for both stages in order for the overall response to cut off at 15 kHz. The second stage required that the z (dampening factor) be set to a certain value. This value is obtained from tables on coefficients of the transfer function for different orders

of filters.

Design:

The transfer function of figure # 2 is as follows:

$$A_{(s)} = [W_c/(s + W_c)] * [(A_oWn^2)/(s^2 + 2zW_ns + W_n^2)]$$

$$= A_oW_cW_n^2/[s^3 + (2zW_n)s^2 + (W_n^2)s + (W_c)s^2 + (2zW_cW_n)s + W_cW_n^2]$$

$$= A_oW_cW_n^2/[s^3 + (2zW_n + W_c)s^2 + (2zW_cW_n + W_n^2)s + W_cW_n^2]$$

To find the magnitude response curve of this filter, jw was substituted into s.

$$A_{(jw)} = A_oW_cW_n^2/[-jw^3 - (2zW_n + W_c)w^2 + j(2zW_cW_n + W_n^2)w + W_cW_n^2]$$

$$M_{(w)} = A_oW_cW_n^2/[(W_cW_n^2 - (2zW_n + W_c)w^2)^2 + ((2zW_cW_n + W_n^2)w - w^3)^2]^{0.5}$$

The cutoff frequency, the natural frequency, the gain and the dampening factor for this filter is...

$A_o = -1$, $z = 0.5$ and $W_c = W_n = 94250$ r/s, therefore the transfer function now becomes:

$$A_{(s)} = 8.3722*10^{14}/(s^3 + 188500s^2 + 1.7766*10^{10}s + 8.3722*10^{14})$$

The third-order filter of figure # 2 consists of two stages. These two stages are:

1. First-order Low-pass Filter.
2. Second-order Low-pass Filter.

1. FIRST-ORDER LOW-PASS FILTER

Theory:

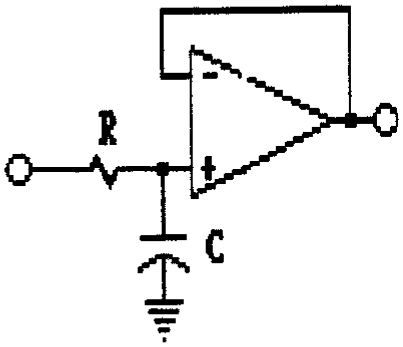


Figure 3. First-order Non-inverting Low-pass Filter.

Figure # 3 which is a first-order non-inverting low-pass filter is configured by R and C. This configuration of R and C produces a cutoff frequency (W_c) determined by the values of R and C.

Design:

The transfer function of figure # 3 is as follows:

$A_{(s)} = W_c/(s + W_c)$

$= (1/sC)/(R + (1/sC)) = 1/(1 + RCs) = (1/RC)/(s +(1/RC))$

Therefore the design equation is:

$W_c = 1/RC \quad ====> \quad 1$

The cutoff frequency and the gain of this filter is...
$A_{(v)} = 1$ and $W_c = 94250$ r/s, therefore the transfer function now becomes:

$A_{(s)} = 94250/(s + 94250)$

Calculating circuit components with W_c set to 1 r/s.

C was assumed to be C = 1 farad, R was calculated using equation # 1.

$R = 1/(C*W_c) = 1/(1*1)$, R = 1 Ω

The cutoff frequency of this filter is $f_c = 15$ kHz.
$w = 2\pi f_c = w = 2*(\pi)*(15*10^3) = 94247.78$ r/s. A frequency

and impedance scaling factor was required to be used to yield practical values of the circuit. K_f and K_z were chosen.

K_f = 94250 r/s

K_z = 2200

Unscaled Components	Scaled Components
R = 1 Ω	R = 2.2 kΩ
C = 1 f	C = 0.004823 μf

The Components Used For Figure # 3 are as Follows:

R = 2.21 kΩ

C = 0.0047 μf

2. SECOND-ORDER LOW-PASS FILTER

Theory:

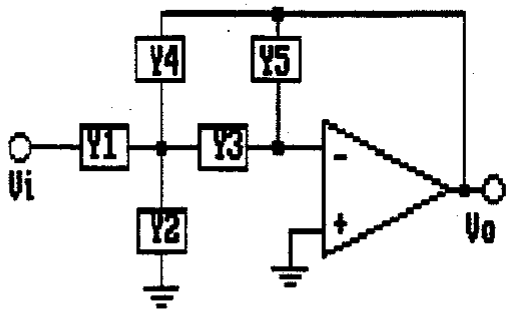


Figure 4. Multiple feedback configuration.

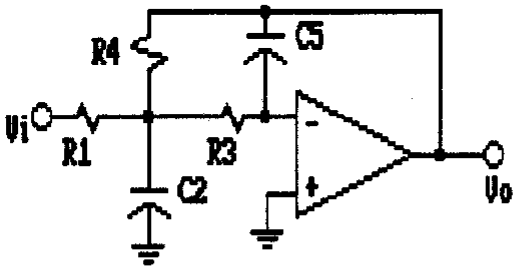


Figure 5. Multiple feedback low-pass filter.

Looking at figure # 4 which is the basis of a multiple feedback circuit using an op-amp (LF347N). By using the proper values for Y1 to Y5, which are admittances, a multiple feedback circuit can be designed to be a low-pass, a high-pass, a bandpass or a band reject filter. In this case a low-pass filter. Y1 to Y5 can be either resistors or capacitors as in figure # 5.

Design:

The transfer function of figure # 5 is as follows:

$$A_{(s)} = (A_o Wn^2)/(s^2 + 2zW_n s + W_n^2)$$

Referring to figure # 4...

$A_{(s)} = -(Y1 * Y3)/[Y5 * (Y1 + Y2 + Y3 + Y4) + Y3Y4]$

$Y1 = 1/R1$, $Y2 = sC2$, $Y3 = 1/R3$, $Y4 = 1/R4$ and $Y5 = sC5$

$A_{(s)} = [-1/(R1 * R3)]/[(C2C5)*s^2 + C5*((1/R1) + (1/R3) + (1/R4))*s + 1/(R3*R4)]$

dividing by C2 * C5

$= (-1/R1R3C2C5)/[s^2 + ((1/C2) * (1/R1 + 1/R3 + 1/R4)) + 1/(R3*R4*C2*C5)]$

Therefore, the three design equations are:

$A_o = -R4/R1 \quad ====> \quad 1,$

$2zW_n = (1/C2)*[(1/R1) + (1/R3) + (1/R4)] \quad ====> \quad 2,$

$W_n^2 = 1/(R3*R4*C2*C5) \quad ====> \quad 3$

The natural frequency, the dampening factor and the gain of this filter is...

$A_{(o)} = -1$, $z = 0.5$ and $W_n = 94250$ r/s, therefore the transfer function now becomes:

$A_{(s)} = 8.883*10^9/(s^2 + 94250s + 8.883*10^9)$

Calculating circuit components with W_n set to 1 r/s.

R4 was assumed to be R4 = 1 Ω, R1 was calculated using equation 1.

$R1 = -R4/-A_o = -1/-1$, R1 = 1 Ω

R3 was assumed to be R3 = 1 Ω, C2 was calculated using equation 2.

C2 = [1/(2*0.5*1)] * (1/1 + 1/1 + 1/1), C2 = 3 farads

C5 was calculated using equation 3.

C5 = 1/[(1)*(1)*(3)*(1)], C5 = 0.3333 farads

It is required that the same frequency scaling factor be used because both first and second order low-pass filters are to cut off at the same frequency. The impedance scaling for both stages can be independent of each other. The impedance scaling was again chosen.

$K_f = 94250$ r/s

$K_z = 1500$

Unscaled components	Scaled Components
R1 = 1 Ω	R1 = 1.5 kΩ
R3 = 1 Ω	R3 = 1.5 kΩ
R4 = 1 Ω	R4 = 1.5 kΩ
C2 = 3 f	C2 = 0.02122 μf
C5 = 0.33333 f	C5 = 0.00236 μf

The Components Used For Figure # 5 is as Follows:

R1 = R3 = R4 = 1.5 kΩ

C2 = 0.022 μf

C5 = 0.0022 μf

Note: The magnitude response curve (graph # 1) of the 15 kHz low-pass filter (calculated and measured) can be found in the results section of this report.

3. TWO-PHASE CLOCK FREQUENCY GENERATOR

Theory:

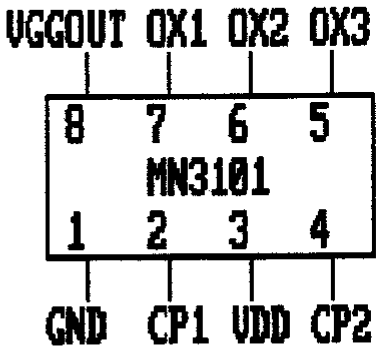


Figure 6. Two-phase Clock Frequency Generator.

The two-phase clock frequency generator (MN3101 - figure # 6) is a CMOS integrated circuit designed to generate low impedance two clock phases required for driving bucket brigade devices (BBD's). Inside of this chip is a self-contained oscillator. This self-contained oscillator can be controlled by an external RC circuit connected to pins 5, 6 and 7. The output clock frequency (CP1 and CP2) is one half the oscillation frequency. Pin number 1 of this chip is grounded as shown on figure # 6. Pin number 2 is clock phase 1 (CP1) which drives all the odd numbered stages and pin number 4 is clock phase 2 (CP2) which drives all the even numbered stages of the bucket brigade device (BBD). Pin number 3 taps off the negative power supply rail of -12 Volts. Pin numbers 5, 6, and 7 (OX3, OX2 and OX1) are for an external RC circuit which determines the frequency of the self-contained oscillator as mentioned previously. Pin

number 8 (VGG OUT-an output pin) is 1 V less than that of the power supply voltage. The relationship between VDD and VGG OUT is VGG OUT = 11/12 VDD.

The clock output, CP1 and CP2 (pins 2 and 4) are 180° out of phase with one another. The output of these pins produce a square wave from 0 volts to -12 volts. These two out of phase square waves are applied to pins 2(CP1) and 6 (CP2) of the BBD.

Design:

When the initial design of the delay circuit was tried, the clock frequency achieved was undesirable. So the components C8, R8, R9 and P6 of the delay circuit (circuit # 2) were adjusted either up or down with reference to the data sheets. P6 controls the clock frequency when it is varied up and down. These components determine the self-contained oscillator frequency. This oscillation frequency is referenced to the data sheets in appendix C.

The Components Used For figure # 6 are as follows:

C8 = 120 pf

R8 = 22.1 kΩ

R9 = 8.2 kΩ

P6 = 50 kΩ

4. BUCKET BRIGADE DEVICE

Theory:

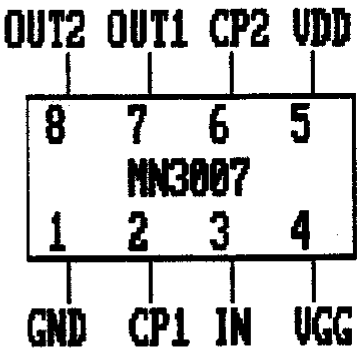


Figure 7. 1024 Stage Bucket Brigade Device.

Figure # 7 is a MN3007 1024-stage long delay Bucket Brigade Device (BBD) that provides a signal delay up to 51.2 milliseconds according to the manufactures specifications. The MN3007 is particularly suitable for use as variable signal delay lines in the audio frequency range. Pin number 1 of the BBD is grounded. Pin number 2 (CP1) which is clock input 1 that connects directly to pin number 2 of figure # 6. Pin number 3 is the audio input pin. According to manufactures specifications, the audio input signal must be riding on -6 volts dc, which is half the supply voltage. P4 of the delay circuit (circuit # 2) controls this bias voltage. Pin number 4 (VDD) gets tied directly to pin number 8 of figure # 6. Pin number 5 is the negative power supply voltage pin. Pin number 6 (CP2) which is clock input 2 which connects directly to pin number 4 of figure # 6. Pins 7 and 8 (delayed output) are output1 and output2.

Design:

With making all connections to both the two-phase clock and the BBD of circuit # 2, the heart of the delay circuit is completed. The two output signals of the BBD are reconstructed together with four resistors R10, R11, R12 and R13 of the delay circuit (circuit # 2). These resistors were arbitrarily selected in reconstructing the two delayed signals. C9 is used to rid the reconstructed output signal of noise. The noise at the output is passed to ground when this capacitor is used. C9 was also arbitrarily selected. C10 is used to couple the output of the BBD to the last circuit element of circuit # 2. The capacitor (C10) is used to block dc voltage.

The last circuit element of the delay circuit (circuit # 2) consists of yet another third-order 15 kHz low-pass filter. This filter is used to filter out any of the clock frequency signal that may appear at the output of the BBD. Therefore the output of this filter contains the reconstructed delayed signal. P5 controls the surround level at the output of this filter. The signal is then routed to a 7 kHz low-pass filter (circuit # 3-appendix A).

The Components Used For Figure # 7 are as Follows:

R10 = R11 = 100 kΩ	C9 = 0.0068 μf
R12 = R13 = 5.62 kΩ	C10 = 2.2 μf

3RD-ORDER 7KHz LOW-PASS FILTER

Theory:

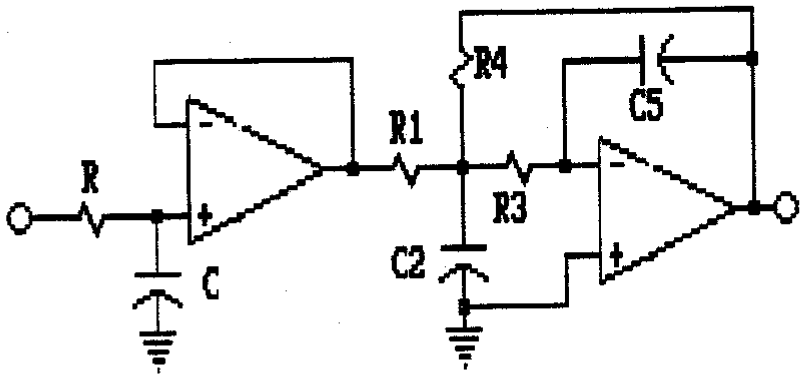


Figure 1. Third-order 7 kHz Low-pass Filter.

The input signal of this filter comes from the centre tap of the pot (P5) from the output of the delay circuit. This pot controls the surround level (amount of delayed signal) that is fed into this filter. This filter (figure # 1) is used for reducing noise even further at its output as compared to the input. High frequencies are also cut out at the output. S2 of circuit # 3-appendix A chooses between the output signal of this filter or the output of the delay circuit (by-pass mode).

Design:

The transfer function of figure # 1 is as follows:

$$A_{(s)} = [W_c/(s + W_c)] * [(A_o Wn^2)/(s^2 + 2zW_n s + W_n^2)]$$

$$= A_o W_c W_n^2/[s^3 + (2zW_n)s^2 + (W_n^2)s + (W_c)s^2 + (2zW_cW_n)s + W_cW_n^2]$$

$$= A_o W_c W_n^2/[s^3 + (2zW_n + W_c)s^2 + (2zW_cW_n + W_n^2)s + W_cW_n^2]$$

To find the magnitude response curve of this filter, jw was substituted into s.

$$A_{(jw)} = A_o W_c W_n^2/[-jw^3 - (2zW_n + W_c)w^2 + j(2zW_cW_n + W_n^2)w + W_cW_n^2]$$

$$M_{(w)} = A_o W_c W_n^2/[(W_cW_n^2 - (2zW_n + W_c)w^2)^2 + ((2zW_cW_n + W_n^2)w - w^3)^2]^{0.5}$$

The cutoff frequency, the natural frequency, the gain and the dampening factor for this filter is...
$A_o = -1$, $z = 0.5$ and $W_c = W_n = 45000$ r/s, therefore the transfer function now becomes:

$$A_{(s)} = 9.1125*10^{13}/(s^3 + 90000s^2 + 4.05*10^9 s + 9.1125*10^{13})$$

The third-order filter of figure # 1 consists of two stages. These two stages are:

1. First-order Low-pass Filter.
2. Second-order Low-pass Filter.

1. FIRST-ORDER LOW-PASS FILTER

Theory:

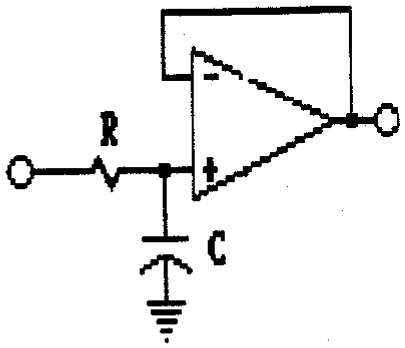


Figure 2. First-Order Non-inverting Low-pass Filter.

Figure # 2 which is a first-order non-inverting low-pass filter is configured by R and C. This configuration of R and C produces a cutoff frequency (W_c) determined by the values of R and C.

Design:

The transfer function of figure # 2 is as follows:

$$A_{(s)} = W_c/(s + W_c)$$

$$= (1/sC)/(R + (1/sC)) = 1/(1 + RCs) = (1/RC)/(s +(1/RC))$$

Therefore the design equation is:

$$W_c = 1/RC \quad ====> \quad 1$$

The cutoff frequency and the gain of this filter is...

$A_{(v)}$ = 1 and W_c = 45000 r/s, therefore the transfer function now becomes:

$A_{(s)}$ = 45000/(s + 45000)

Calculating circuit components with W_c set to 1 r/s.

C was assumed to be C = 14 farads, R was calculated using equation # 1.

R = 1/(C*W_c) = 1/(14*1), R = 0.07142857 Ω

The cutoff frequency of this filter is f_c = 7 kHz.

w = 2πf_c = w = 2*(π)*(7*10^3) = 43982.297 r/s. A frequency and impedance scaling factor was required to be used to yield practical values of the circuit. K_f and K_z were chosen.

K_f = 45000 r/s

K_z = 15000

Unscaled Components	Scaled Components
R = 0.07142857 Ω	R = 1071.428571 Ω
C = 14 f	C = 0.02074 μf

The Components Used For Figure # 2 are as Follows:

R = 1 kΩ

C = 0.022 μf

2. SECOND-ORDER LOW-PASS FILTER

Theory:

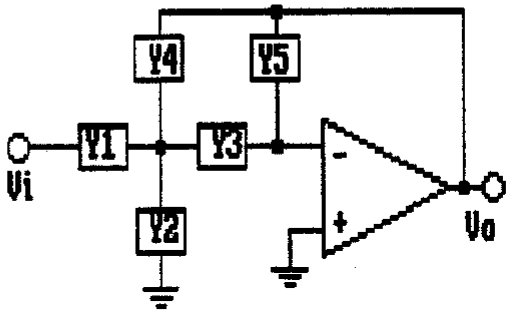


Figure 3. Multiple feedback configuration.

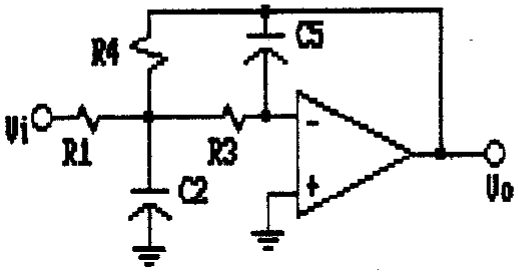


Figure 4. Multiple feedback low-pass filter.

The theory for figures 3 and 4 are the same as the second-order low-pass filter explained in the design section of the 15 kHz low-pass filter of the delay circuit (circuit # 2-appendix A).

Design:

The transfer function of figure # 4 is as follows:

$$A_{(s)} = (A_o Wn^2)/(s^2 + 2zW_n s + W_n^2)$$

Referring to figure # 3...

$A_{(s)} = -(Y1 * Y3)/[Y5 * (Y1 + Y2 + Y3 + Y4) + Y3Y4]$

$Y1 = 1/R1$, $Y2 = sC2$, $Y3 = 1/R3$, $Y4 = 1/R4$ and $Y5 = sC5$

$A_{(s)} = [-1/(R1 * R3)]/[(C2C5)*s^2 + C5*((1/R1) + (1/R3) + (1/R4))*s + 1/(R3*R4)]$

dividing by C2 * C5

$= (-1/R1R3C2C5)/[s^2 + ((1/C2) * (1/R1 + 1/R3 + 1/R4)) + 1/(R3*R4*C2*C5)]$

Therefore, the three design equations are:

$A_o = -R4/R1$ ====> 1,

$2zW_n = (1/C2)*[(1/R1) + (1/R3) + (1/R4)]$ ====> 2,

$W_n^2 = 1/(R3*R4*C2*C5)$ ====> 3

The natural frequency, the dampening factor and the gain of this filter is...

$A_{(o)} = -1$, $z = 0.5$ and $W_n = 45000$ r/s, therefore the transfer function now becomes:

$A_{(s)} = 2.025*10^9/(s^2 + 45000s + 2.025*10^9)$

Calculating circuit components with W_n set to 1 r/s.

R4 was assumed to be R4 = 1 Ω, R1 was calculated using equation 1.

$R1 = -R4/-A_o = -1/-1$, R1 = 1 Ω

R3 was assumed to be R3 = 1 Ω, C2 was calculated using equation 2.

$C2 = [1/(2*0.5*1)] * (1/1 + 1/1 + 1/1)$, C2 = 3 farads

C5 was calculated using equation 3.

$C5 = 1/[(1)*(1)*(3)*(1)]$, C5 = 0.3333 farads

It is required that the same frequency scaling factor be used because both first and second order low-pass filters are to cut off at the same frequency. The impedance scaling for both stages can be independent of each other. The impedance scaling was again chosen.

$K_f = 45000$ r/s

$K_z = 1500$

Unscaled components	Scaled Components
R1 = 1 Ω	R1 = 1.5 kΩ
R3 = 1 Ω	R3 = 1.5 kΩ
R4 = 1 Ω	R4 = 1.5 kΩ
C2 = 3 f	C2 = 0.04444 μf
C5 = 0.33333 f	C5 = 0.00494 μf

The Components Used For Figure # 4 are as Follows:

R1 = R3 = R4 = 1.5 kΩ

C2 = 0.047 μf

C5 = 0.0047 μf

The output signal of the 7 kHz low-pass filter (figure # 1) is applied to the left channel of the power amplifier. The same output signal is inverted as shown in circuit # 3 of appendix A and applied to the right channel of the power amplifier. This power amplifier drives a pair of speakers located to the rear of the listener.

Note: The magnitude response curve (graph # 2) of this filter (calculated and measured) can be found in the results section of this report.

CENTRE CHANNEL BANDPASS FILTER

Theory:

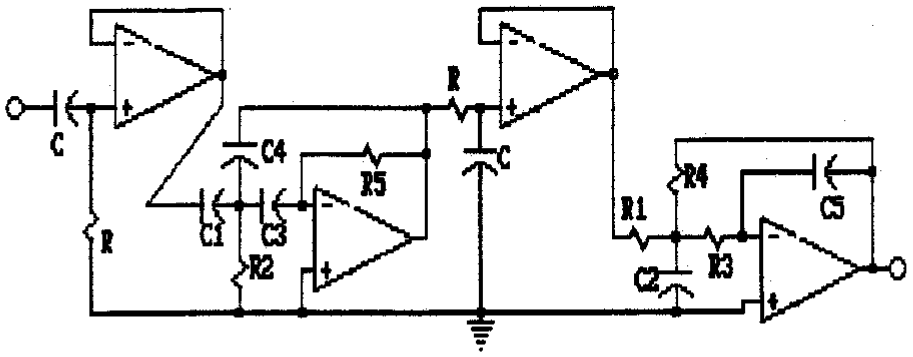


Figure 1. Third-order Bandpass Filter.

The purpose of this centre channel bandpass filter (figure # 1) is to rid the summation signal of high and low frequencies. The bandpass filter's half power frequencies are 300 Hz and 3000 Hz respectively. The bandwidth of this filter is 2700 Hz, which is all the common mid-range frequencies. This bandpass filter is made up of a third-order low-pass filter (figure # 2) and a third-order high-pass filter (figure # 6). The cutoff frequency of the third-order low-pass filter is 3 kHz and the cutoff frequency of the third-order high-pass filter is 300 Hz. When these two filters (figures 1 and 6) are cascaded together they form a bandpass filter as shown in circuit # 4-appendix A. The output signal of this bandpass filter is speech (mid-range frequencies).

The third-order filter of figure # 1 consists of two stages. These two stages are:

1. Third-Order Low-pass Filter.
2. Third-Order High-pass Filter.

1. THIRD-ORDER LOW-PASS FILTER

Theory:

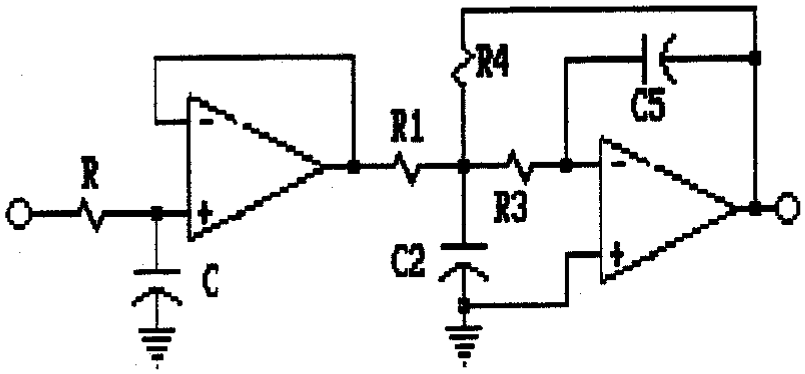


Figure 2. Third-order 3 kHz Low-pass Filter.

This filter is used the second section of the third-order bandpass filter (figure # 1). The first stage is of a first-order non-inverting low-pass filter. The second stage is of a second-order inverting low-pass filter. When both stages are put together, it forms a third-order 3 kHz low-pass filter. In designing a third-order low-pass filter, it is a requirement to make both stages cut off at the same frequency. In other words the frequency scaling factor is required to be the same for both stages in order for the

overall response to cut off at 3 kHz. The second stage required that the z (dampening factor) be set to a certain value. This value is obtained from tables on coefficients of the transfer function for different orders of filters.

Design:

The transfer function of figure # 2 is as follows:

$$A_{(s)} = [W_c/(s + W_c)] * [(A_o Wn^2)/(s^2 + 2zW_n s + W_n^2)]$$

$$= A_o W_c W_n^2/[s^3 + (2zW_n)s^2 + (W_n^2)s + (W_c)s^2 + (2zW_c W_n)s + W_c W_n^2]$$

$$= A_o W_c W_n^2/[s^3 + (2zW_n + W_c)s^2 + (2zW_c W_n + W_n^2)s + W_c W_n^2]$$

To find the magnitude response curve of this filter, jw was substituted into s.

$$A_{(jw)} = A_o W_c W_n^2/[-jw^3 - (2zW_n + W_c)w^2 + j(2zW_c W_n + W_n^2)w + W_c W_n^2]$$

$$M_{(w)} = A_o W_c W_n^2/[(W_c W_n^2 - (2zW_n + W_c)w^2)^2 + ((2zW_c W_n + W_n^2)w - w^3)^2]^{0.5}$$

The cutoff frequency, the natural frequency, the gain and the dampening factor for this filter are...

$A_o = -1$, $z = 0.5$ and $W_c = W_n = 19000$ r/s, therefore the transfer function now becomes:

$$A_{(s)} = 6.859*10^{12}/(s^3 + 38000s^2 + 7.22*10^8s + 6.859*10^{12})$$

The third-order filter of figure # 2 consists of two stages. These two stages are:

1. First-order Low-pass Filter.
2. Second-order Low-pass Filter.

1. FIRST-ORDER LOW-PASS FILTER

Theory:

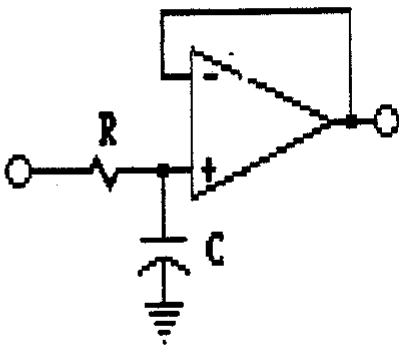


Figure 3. First-Order Non-inverting Low-pass Filter.

Figure # 2 which is a first-order non-inverting low-pass filter is configured by R and C. This configuration of R and C produces a cutoff frequency (W_c) determined by the values of R and C.

Design:

The transfer function of figure # 3 is as follows:

$A_{(s)} = W_c/(s + W_c)$

$= (1/sC)/(R + (1/sC)) = 1/(1 + RCs) = (1/RC)/(s +(1/RC))$

Therefore the design equation is:

$W_c = 1/RC \quad ====> \quad 1$

The cutoff frequency and the gain of this filter is...
$A_{(v)} = 1$ and $W_c = 19000$ r/s, therefore the transfer function now becomes:

$A_{(s)} = 19000/(s + 19000)$

Calculating circuit components with W_c set to 1 r/s.

C was assumed to be C = 1 farad, R was calculated using equation # 1.

$R = 1/(C*W_c) = 1/(1*1)$, R = 1 Ω

The cutoff frequency of this filter is f_c = 3000 Hz. $w = 2\pi f_c$ = w = 2*(π)*(3000) = 18849.556 r/s. A frequency and impedance scaling factor was required to be used to yield practical values of the circuit. K_f and K_z were chosen.

K_f = 19000 r/s

K_z = 2400

Unscaled Components	Scaled Components
R = 1 Ω	R = 2.4 kΩ
C = 1 f	C = 0.02193 μf

The Components Used For Figure # 2 are as Follows:

R = 2.4 kΩ

C = 0.022 μf

2. SECOND-ORDER LOW-PASS FILTER

Theory:

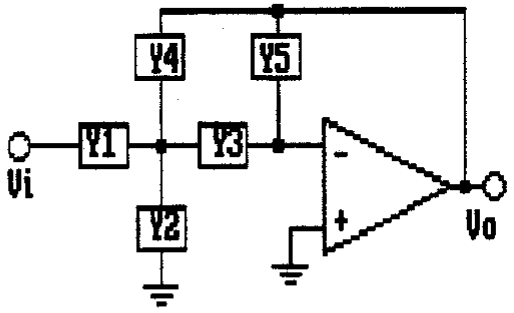


Figure 4. Multiple feedback configuration.

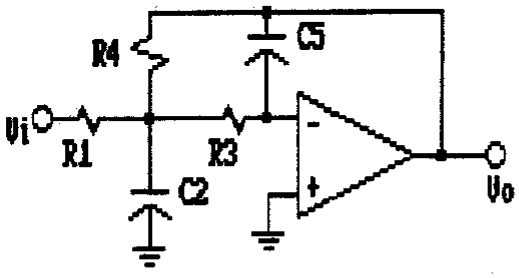


Figure 5. Multiple feedback low-pass filter.

The theory for figures 4 and 5 are the same as the second-order low-pass filter explained in the design section of the 15 kHz low-pass filter of the delay circuit (circuit # 2-appendix A).

Design:

The transfer function of figure # 5 is as follows:

$$A_{(s)} = (A_o Wn^2)/(s^2 + 2zW_n s + W_n^2)$$

Referring to figure # 4...

$$A_{(s)} = -(Y1 * Y3)/[Y5 * (Y1 + Y2 + Y3 + Y4) + Y3Y4]$$

Y1 = 1/R1, Y2 = sC2, Y3 = 1/R3, Y4 = 1/R4 and Y5 = sC5

$A_{(s)} = [-1/(R1 * R3)]/[(C2C5)*s^2 + C5*((1/R1) + (1/R3) + (1/R4))*s + 1/(R3*R4)]$

dividing by C2 * C5

$= (-1/R1R3C2C5)/[s^2 + ((1/C2) * (1/R1 + 1/R3 + 1/R4)) + 1/(R3*R4*C2*C5)]$

Therefore, the three design equations are:

$A_o = -R4/R1 \quad ====> \quad 1,$

$2zW_n = (1/C2)*[(1/R1) + (1/R3) + (1/R4)] \quad ====> \quad 2,$

$W_n^2 = 1/(R3*R4*C2*C5) \quad ====> \quad 3$

The natural frequency, the dampening factor and the gain of this filter is...

$A_{(o)} = -1$, $z = 0.5$ and $W_n = 19000$ r/s, therefore the transfer function now becomes:

$A_{(s)} = 3.61*10^8/(s^2 + 19000s + 3.61*10^8)$

Calculating circuit components with W_n set to 1 r/s.

R4 was assumed to be <u>R4 = 1 Ω</u>, R1 was calculated using equation # 1.

R1 = -1/-1, <u>R1 = 1 Ω</u>

R3 was assumed to be R3 = 1 Ω, C2 was calculated using equation # 2.

C2 = [1/(2*0.5*1)] * (1/1 + 1/1 + 1/1), C2 = 3 farads

C5 was calculated using equation # 3.

C5 = 1/[(1)*(1)*(3)*(1)], C5 = 0.33333 farads

It is required that the same frequency scaling factor be used because both first and second order low-pass filters are to cut off at the same frequency. The impedance scaling for both stages can be independent of each other. The impedance scaling was again chosen.

K_f = 19000 r/s

K_z = 2210

Unscaled components	Scaled Components
R1 = 1 Ω	R1 = 2.21 kΩ
R3 = 1 Ω	R3 = 2.21 kΩ
R4 = 1 Ω	R4 = 2.21 kΩ
C2 = 3 f	C2 = 0.07145 μf
C5 = 0.33333 f	C5 = 0.00794 μf

The Components Used For Figure # 5 is as Follows:

R1 = R3 = R4 = 2.21 kΩ

C2 = 0.068 μf

C5 = 0.0068 μf

2. THIRD-ORDER HIGH-PASS FILTER

Theory:

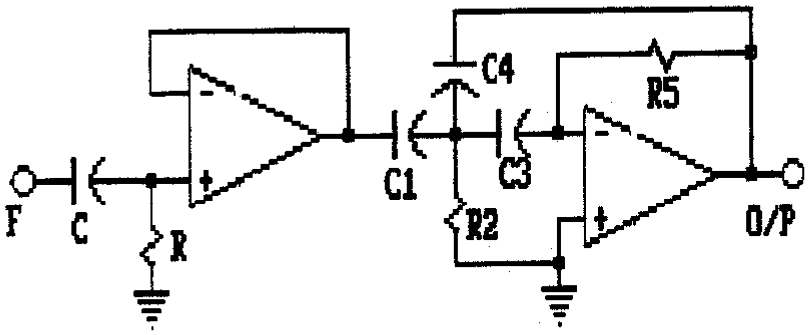


Figure 6. Third-Order High-pass Filter.

The third-order 300 Hz high-pass filter is similar to that used for a low-pass filter. It can be shown that the component configuration of the high-pass filter circuit (figure # 6) are opposite that of the low-pass filter (figure # 2). This filter is found in the first section of the third-order bandpass filter (figure # 1). The first stage is of a first-order non-inverting high-pass filter. The second stage is of a second-order inverting high-pass filter.

Design:

The transfer function of figure # 6 is as follows:

$$A_{(s)} = [s/(s + W_c)] * [(A_\infty s^2)/(s^2 + 2zW_n s + W_n^2)]$$

$$= A_\infty s^3/[s^3 + (2zW_n)s^2 + (W_n^2)s + (W_c)s^2 + (2zW_cW_n)s + W_cW_n^2]$$

$$= A_\infty s^3/[s^3 + (2zW_n + W_c)s^2 + (2zW_cW_n + W_n^2)s + W_cW_n^2]$$

To find the magnitude response curve of this filter, jw was substituted into s.

$$A_{(jw)} = A_\infty -jw^3/[-jw^3 - (2zW_n + W_c)w^2 + j(2zW_cW_n + W_n^2)w + W_cW_n^2]$$

$$M_{(w)} = A_\infty w^3/[(W_cW_n^2 - (2zW_n + W_c)w^2)^2 + ((2zW_cW_n + W_n^2)w - w^3)^2]^{0.5}$$

The cutoff frequency, the natural frequency, the gain and the dampening factor for this filter is...

$A_o = -1$, $z = 0.5$ and $W_c = W_n = 2000$ r/s, therefore the transfer function now becomes:

$$A_{(s)} = A_\infty s^3/(s^3 + 4000s^2 + 8*10^6 s + 8*10^9)$$

The third-order filter of figure # 6 consists of two stages. These two stages are:

1. First-order High-pass Filter.
2. Second-order High-pass Filter.

1. FIRST-ORDER HIGH-PASS FILTER

Theory:

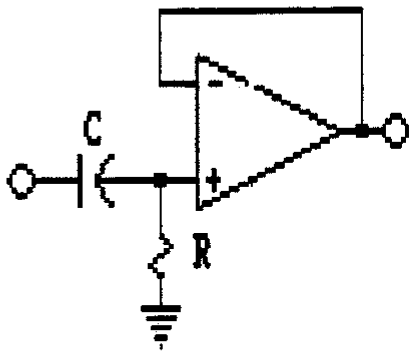


Figure 7. First-Order High-pass Filter.

Figure # 7 which is a first-order non-inverting high-pass filter is configured by R and C. This configuration of R and C produces a cutoff frequency (W_c) determined by the values of R and C.

Design:

The transfer function of figure # 7 is as follows:

$$A_{(s)} = s/(s + W_c)$$

Therefore the design equation is:

$W_c = 1/RC \quad ====> \quad 1$

The cutoff frequency and the gain of this filter is... $A_{(v)} = 1$ and $W_c = 2000$ r/s, therefore the transfer function now becomes:

$A_{(s)} = s/(s + 2000)$

Calculating circuit components with W_c set to 1 r/s.

C was assumed to be <u>C = 1 farad</u>, R was calculated using equation # 1.

$R = 1/(C*W_c) = 1/(1*1)$, <u>R = 1 Ω</u>

The cutoff frequency of this filter is $f_c = 300$ Hz. $w = 2\pi f_c = w = 2*(\pi)*(300) = 1884.956$ r/s. A frequency and impedance scaling factor was required to be used to yield practical values of the circuit. K_f and K_z were chosen.

$K_f = 2000$ r/s

$K_z = 22100$

Unscaled Components	Scaled Components
R = 1 Ω	R = 22.1 kΩ
C = 1 f	C = 0.02262 μf

The Components Used For Figure # 7 are as Follows:

R = 22.1 kΩ

C = 0.022 μf

2. SECOND-ORDER HIGH-PASS FILTER

Theory:

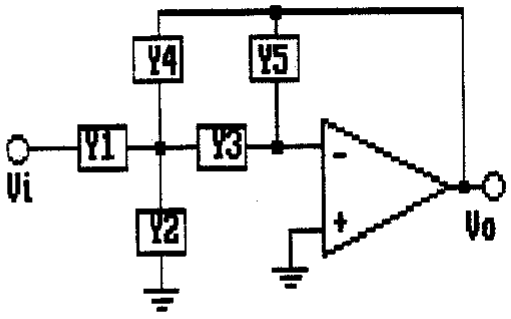


Figure 8. Multiple feedback configuration.

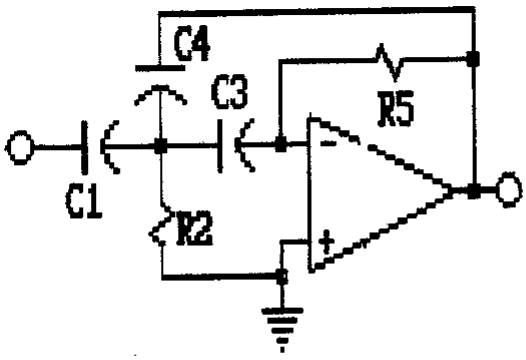


Figure 9. Second-order High-pass Filter.

The theory for figures 8 and 9 are the same as the second-order low-pass filter explained earlier in this section.

Design:

The transfer function of figure # 9 is as follows:

$$A_{(s)} = (A_\infty s^2)/(s^2 + 2zW_n s + W_n^2)$$

Referring to figure # 8...

$$A_{(s)} = -(Y1 * Y3)/[Y5 * (Y1 + Y2 + Y3 + Y4) + Y3Y4]$$

$Y1 = sC1$, $Y2 = 1/R2$, $Y3 = sC3$, $Y4 = sC4$ and $Y5 = 1/R5$

$$A_{(s)} = -s^2C1C3/[((1/R5)*(sC1 + 1/R2 + sC3 + sC4)) + s^2C3C4]$$

dividing by C3 * C4

$$= (-C1/C4)s^2/[s^2 + ((1/R5)*(C1/C3C4 + 1/C3 + 1/C4) + 1/R2R5C3C4]$$

Therefore, the three design equations are:

$A_\infty = -C1/C4$ ====> 1,

$2zW_n = (1/R5)*(C1/C3C4 + 1/C3 + 1/C4)$ ====> 2,

$W_n^2 = 1/(R2*R5*C3*C4)$ ====> 3

The natural frequency, the dampening factor and the gain of this filter is...

$A_{(\infty)} = -1$, $z = 0.5$ and $W_n = 2000$ r/s, therefore the transfer function now becomes:

$$A_{(s)} = s^2/(s^2 + 2000s + 4*10^6)$$

Calculating circuit components with W_n set to 1 r/s.

C1 was assumed to be C1 = 1 farad, C4 was calculated using equation # 1.

C4 = -1/-1, C4 = 1 farad

C3 was assumed to be C3 = 1 farad, R5 was calculated using equation # 2.

R5 = (1/(2*0.5*1))*(1/(1*1) + 1/1 + 1/1), R5 = 3 Ω

R2 was calculated using equation # 3.

R2 = 1/(1*3*1*1), R2 = 0.33333 Ω

It is required that the same frequency scaling factor be used because both first and second order high-pass filters are to cut off at the same frequency. The impedance scaling for both stages can be independent of each other. The impedance scaling was again chosen.

K_f = 2000 r/s

K_z = 16900

Unscaled components	Scaled Components
R2 = 0.3333 Ω	R2 = 5.6333 kΩ
R5 = 3 Ω	R5 = 50.7 kΩ
C1 = 1 f	C1 = 0.02959 μf
C3 = 1 f	C3 = 0.02959 μf
C4 = 1 f	C4 = 0.02959 μf

The Components Used For Figure # 9 are as Follows:

R2 = 5.62 kΩ

R5 = 39.2 kΩ

C1 = C3 = C4 = 0.033 μf

Note: The magnitude response curve (graph # 3) of this filter (calculated and measured) can be found in the results section of this report.

$$= A_o W_c W_n^2/[s^3 + (2zW_n)s^2 + (W_n^2)s + (W_c)s^2 + (2zW_cW_n)s + W_cW_n^2]$$

$$= A_o W_c W_n^2/[s^3 + (2zW_n + W_c)s^2 + (2zW_cW_n + W_n^2)s + W_cW_n^2]$$

To find the magnitude response curve of this filter, jw was substituted into s.

$$A_{(jw)} = A_o W_c W_n^2/[-jw^3 - (2zW_n + W_c)w^2 + j(2zW_cW_n + W_n^2)w + W_cW_n^2]$$

$$M_{(w)} = A_o W_c W_n^2/[(W_cW_n^2 - (2zW_n + W_c)w^2)^2 + ((2zW_cW_n + W_n^2)w - w^3)^2]^{0.5}$$

The cutoff frequency, the natural frequency, the gain and the dampening factor for this filter is...
$A_o = -1$, $z = 0.5$ and $W_c = W_n = 500$ r/s, therefore the transfer function now becomes:

$$A_{(s)} = 1.25*10^8/(s^3 + 1000s^2 + 500*10^3s + 1.25*10^8)$$

The third-order filter of figure # 1 consists of two stages. These two stages are:

1. First-order Low-pass Filter.
2. Second-order Low-pass Filter.

1. FIRST-ORDER LOW-PASS FILTER

Theory:

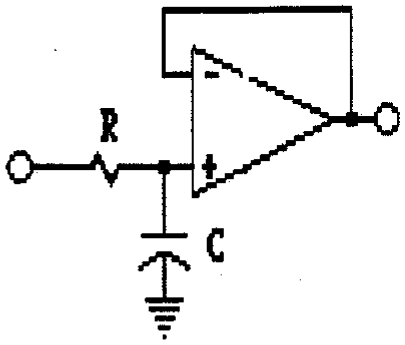


Figure 2. First-Order Non-inverting Low-pass Filter.

Figure # 2 which is a first-order non-inverting low-pass filter is configured by R and C. This configuration of R and C produces a cutoff frequency (W_c) determined by the values of R and C.

Design:

The transfer function of figure # 2 is as follows:

$$A_{(s)} = W_c/(s + W_c)$$

$$= (1/sC)/(R + (1/sC)) = 1/(1 + RCs) = (1/RC)/(s +(1/RC))$$

Therefore the design equation is:

$$W_c = 1/RC \quad ====> \quad 1$$

The cutoff frequency and the gain of this filter is...
$A_{(v)}$ = 1 and W_c = 500 r/s, therefore the transfer function now becomes:

$A_{(s)} = 500/(s + 500)$

Calculating circuit components with W_c set to 1 r/s.

C was assumed to be C = 1 farad, R was calculated using equation 1.

$R = 1/(C*W_c) = 1/(14*1)$, R = 1 Ω

The cutoff frequency of this filter is f_c = 75 Hz.
$w = 2\pi f_c = w = 2*(\pi)*(75) = 471.239$ r/s. A frequency and impedance scaling factor was required to be used to yield practical values of the circuit. K_f and K_z were chosen.

K_f = 500 r/s
K_z = 20000

Unscaled Components	Scaled Components
R = 1 Ω	R = 20 kΩ
C = 1 f	C = 0.1 μf

The Components Used For Figure # 2 are as Follows:

R = 20 kΩ

C = 0.1 μf

2. SECOND-ORDER LOW-PASS FILTER

Theory:

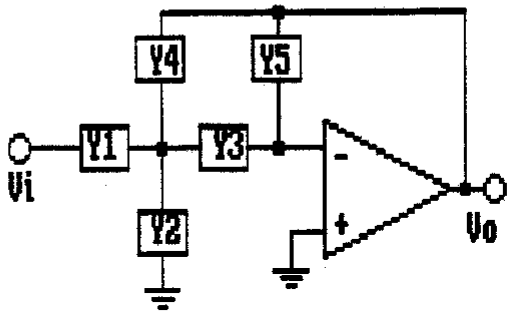


Figure 3. Multiple feedback configuration.

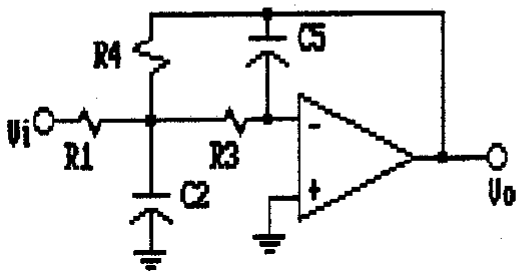


Figure 4. Multiple feedback low-pass filter.

The theory for figures 3 and 4 are the same as the second-order low-pass filter explained in the design section of the 15 kHz low-pass filter of the delay circuit (circuit # 2-appendix A).

Design:

The transfer function of figure # 4 is as follows:

$$A_{(s)} = (A_o Wn^2)/(s^2 + 2zW_n s + W_n^2)$$

Referring to figure # 3...

$A_{(s)} = -(Y1 * Y3)/[Y5 * (Y1 + Y2 + Y3 + Y4) + Y3Y4]$

$Y1 = 1/R1$, $Y2 = sC2$, $Y3 = 1/R3$, $Y4 = 1/R4$ and $Y5 = sC5$

$A_{(s)} = [-1/(R1 * R3)]/[(C2C5)*s^2 + C5*((1/R1) + (1/R3) + (1/R4))*s + 1/(R3*R4)]$

dividing by C2 * C5

$= (-1/R1R3C2C5)/[s^2 + ((1/C2) * (1/R1 + 1/R3 + 1/R4)) + 1/(R3*R4*C2*C5)]$

Therefore, the three design equations are:

$A_o = -R4/R1 \quad ====> \quad 1,$

$2zW_n = (1/C2)*[(1/R1) + (1/R3) + (1/R4)] \quad ====> \quad 2,$

$W_n^2 = 1/(R3*R4*C2*C5) \quad ====> \quad 3$

The natural frequency, the dampening factor and the gain of this filter is...

$A_{(o)} = -1$, $z = 0.5$ and $W_n = 500$ r/s, therefore the transfer function now becomes:

$A_{(s)} = 250*10^3/(s^2 + 500s + 250*10^3)$

Calculating circuit components with W_n set to 1 r/s.

R4 was assumed to be R4 = 0.2 Ω, R1 was calculated using equation 1

$R1 = -R4/-A_o = -1/-1$, R1 = 0.2 Ω

R3 was assumed to be R3 = 1 Ω, C2 was calculated using equation 2.

$C2 = [1/(2*0.5*1)] * (1/1 + 1/1 + 1/1)$, C2 = 11 farads

C5 was calculated using equation 3.

$C5 = 1/[(1)*(1)*(3)*(1)]$, C5 = 0.454545 farads

It is required that the same frequency scaling factor be used because both first and second order low-pass filters are to cut off at the same frequency. The impedance scaling for both stages can be independent of each other. The impedance scaling was again chosen.

$K_f = 500$ r/s

$K_z = 100000$

Unscaled components	Scaled Components
R1 = 0.2 Ω	R1 = 20 kΩ
R3 = 1 Ω	R3 = 100 kΩ
R4 = 0.2 Ω	R4 = 20 kΩ
C2 = 11 f	C2 = 0.22 μf
C5 = 0.454545 f	C5 = 0.0090909 μf

The Components Used For Figure # 4 are as Follows:

R1 = R4 = 20 kΩ

R3 = 100 kΩ

C2 = 0.22 μf

C5 = 0.01 μf

INVERTING SUMMING AMPLIFIER

Theory:

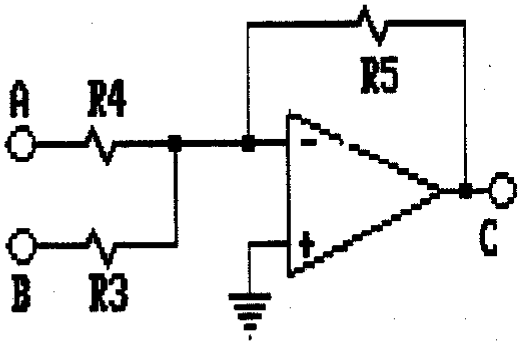


Figure 5. An Inverting Summing Amplifier.

Figure # 5 which an inverting summing amplifier, summs the input left and right signals together. Point A is the input signal from the left channel buffer and point B is the input signal from the right channel buffer. After both input signals have been summed together, the summated signal is inverted by 180°. This provides a low driving impedance for the low-pass filter (figure # 1). If either R3 or R4 were changed, there would not be equal amounts of input signals being summed together. So having these resistors the same is essential.

Design:

$V_{oa} = (R5/R4)*A \quad ====> \quad 1$

$V_{ob} = (R5/R3)*B \quad ====> \quad 2$

The output voltage V_o is...

$V_o = V_{oa} + V_{ob}$

$V_o = ((R5/R4)*A + (R5/R3)*B) \quad ====> \quad 3$

R4 and R3 were assumed with reference to equation # 3. R5 controls the overall output voltage. R5 was also assumed.

The Components Used For Figure # 5 are as Follows:

R3 = R4 = 47.5 kΩ

R5 = 100 kΩ

The output of the third-order 75 Hz low-pass filter is controlled by P3 (subwoofer level) of circuit # 5-appendix A. Subwoofer levels at the output can be varied up or down by this pot. This output subwoofer signal drives a subwoofer amplifier for base response. Adding low frequency sounds to the overall system.

Note: The magnitude response curve (graph # 4) of this filter (calculated and measured) can be found in the results section of this report.

RESULTS

Signal Processing Circuit

When the signal processing circuit was constructed, a sinusoidal waveform (1 Vp-p) was applied to the right channel input buffer. One output was scoped at pin # 1 of IC2-a and the other at pin # 1 of IC2-b. The output waveform IC2-a was of a sinusoidal waveform. When P1 was varied up to its maximum, the output voltage increased to 3 Vp-p, which was expected (gain of times 3). When P1 was varied to zero, the output voltage was 1 Vp-p (gain of times 1). The output of IC2-b was a sinusoidal waveform with a voltage of 1.6 Vp-p.

The left WIDE production circuit (IC2-c) was also scoped. The output of this production circuit was under 1 Vp-p when the frequency of the input sinewave was below 34 Hz (the cutoff frequency of IC2-c-d). When the input frequency was increased above 34 Hz, the output remained at 1 Vp-p at any frequency above this cutoff frequency of 34 Hz. The output of IC2-d was exactly the same when the input sinewave was applied to the opposite input buffer.

Delay Circuit

The magnitude response curve of the third-order 15 kHz low-pass filter of this delay circuit can be found on page 78. The measured response curve is a little bit less than that of the calculated response curve as shown. The response of this filter turned out exceptionally well with no major differences.

The clock outputs of the MN3101 two-phase clock frequency generator were measured. The output waveform of pins 2 and 4 is a square wave with a voltage of 0 V to -12 V. These two output waveforms are 180° out of phase with one another. When P6 was varied up and down the clock frequency changed.

Minimum clock frequency = 26.749 kHz

Maximum clock frequency = 120.977 kHz

These minimum and maximum frequencies are the same at both pins 2 and 4. Since minimum and maximum clock frequencies are known, the minimum and maximum delays can be found.

Delay = # of stages of the BBD/(2 * the clock frequency)

maximum delay = $1024/(2*26.749*10^3)$ = 19.141 milliseconds

minimum delay = $1024/(2*120.977*10^3)$ = 4.232 milliseconds

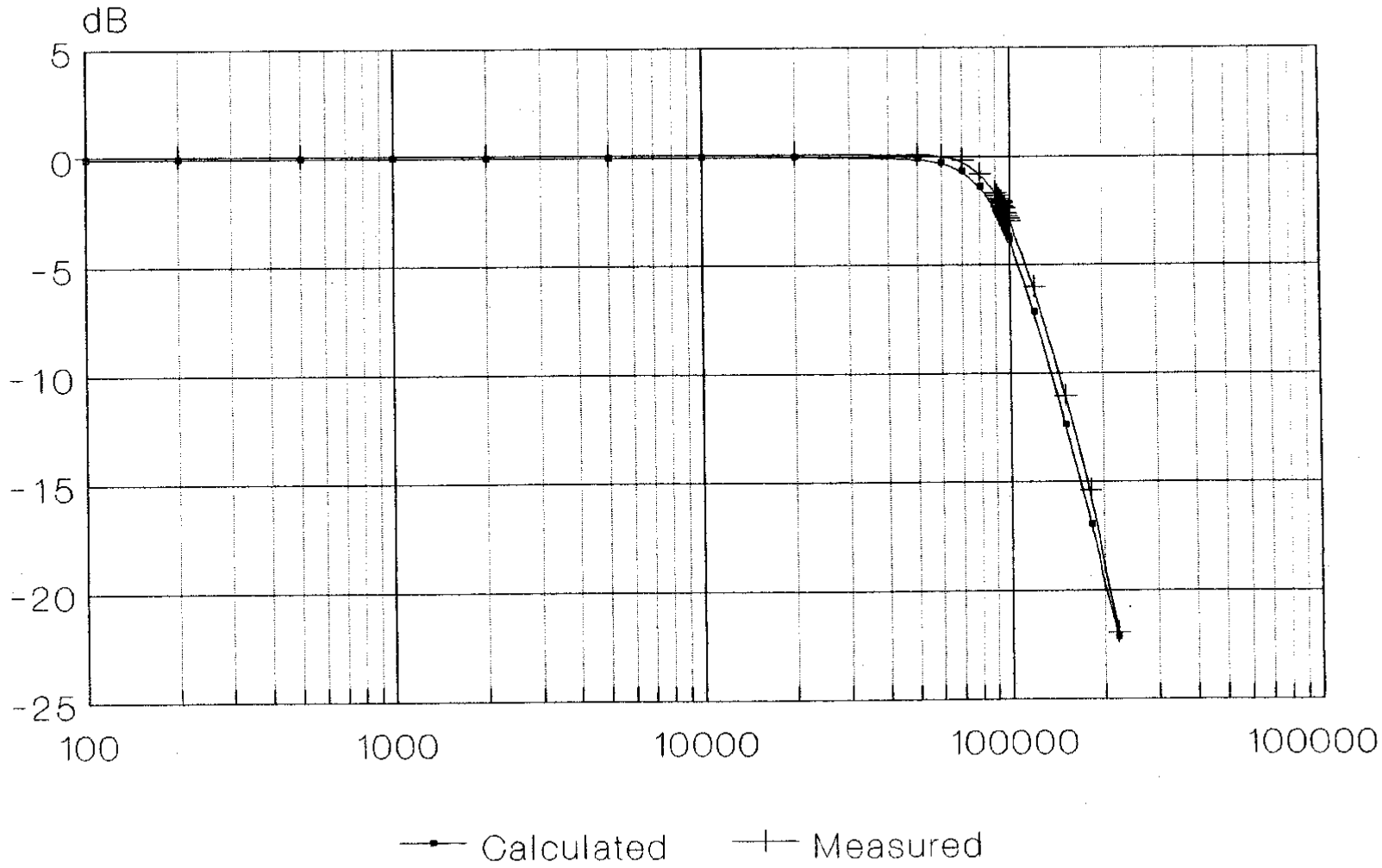
The voltage at pin 3 was measured to be -6.2 V.

The pot (P4) varies the bias voltage to this input pin. A requirement of the BBD is to have half the supply voltage at this pin. This was accomplished. Pins 7 and 8 are the output pins of the BBD. The output delayed signal of each individual pin are combined to form a signal similar to the input signal but only delayed. This delayed signal can be shown on the oscilloscope. If channel one on the oscilloscope is triggered by the input signal (at pin 3) and the delayed signal (output combined of the BBD) is applied to channel two and P6 varied, the signal seen on the scope from channel two moves across the screen. This action can only be seen if the scope is triggered on channel one.

Filter Response

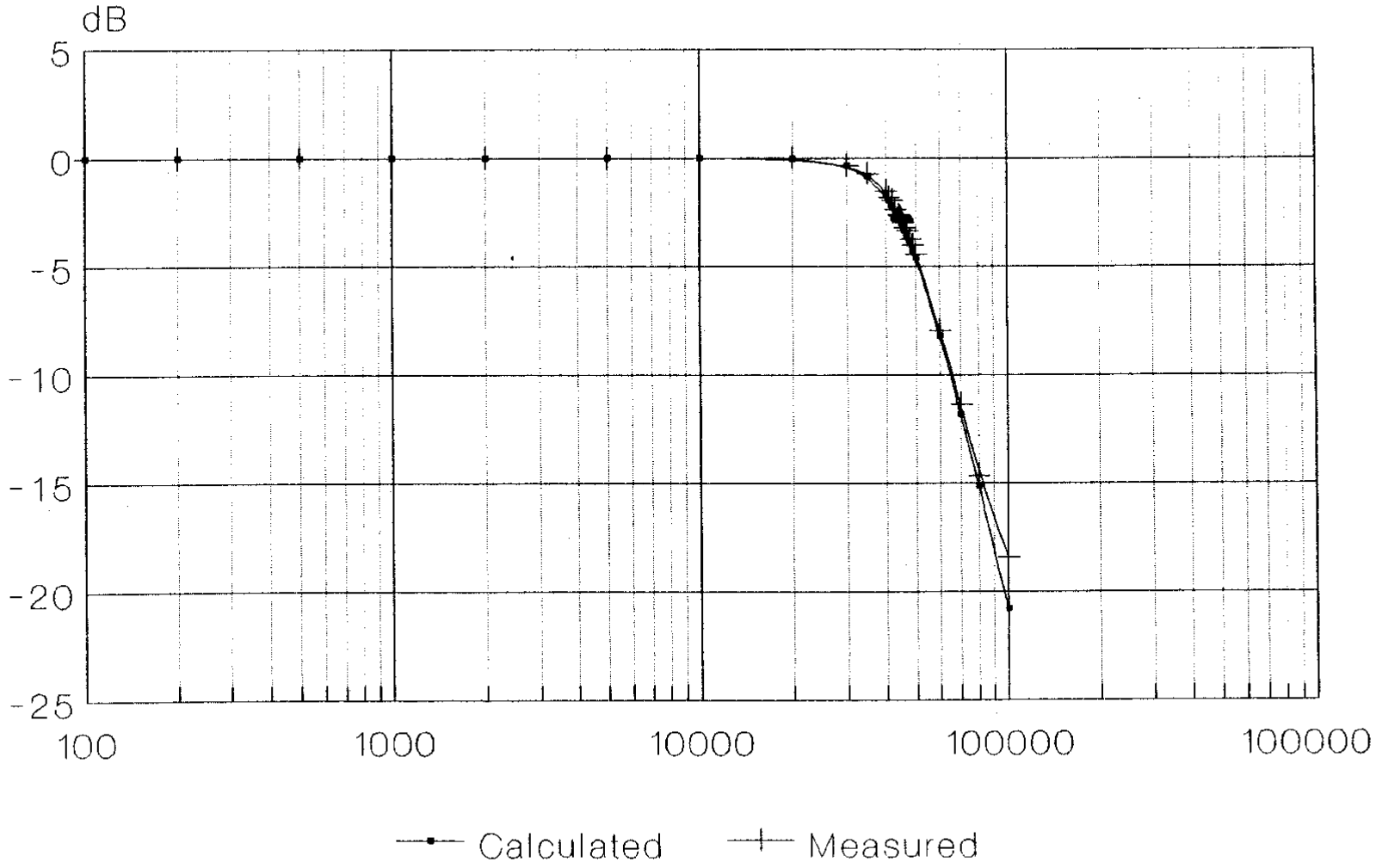
The response curves of the 7 kHz low-pass-75 Hz low-pass and 300-3000 Hz bandpass filters are found on the preceding pages (pgs 79,80 and 81). The response of each of these filters turned out very well. There are no major differences.

Magnitude Response



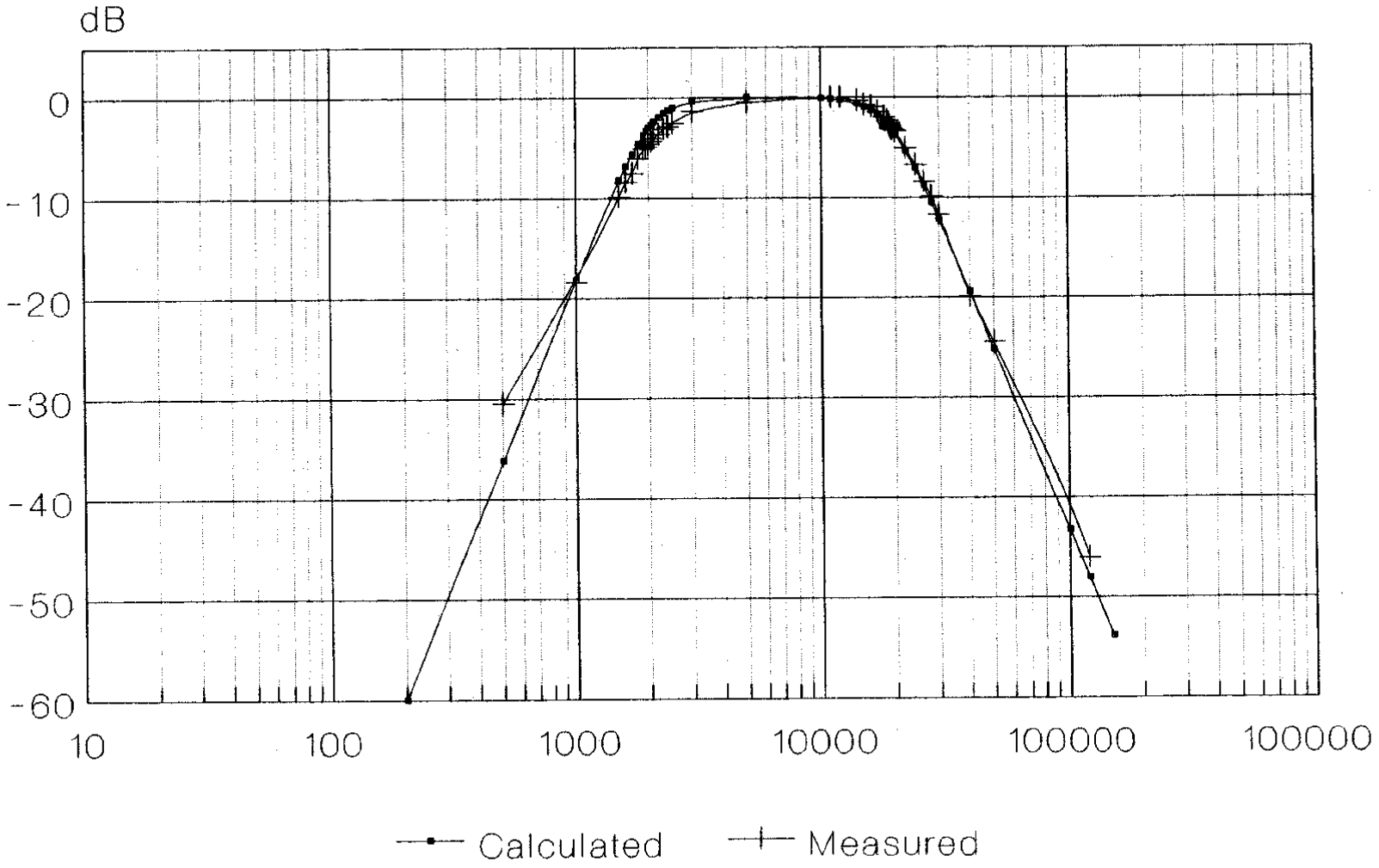
Graph 1. 15 kHz Low-pass Filter

Magnitude Response



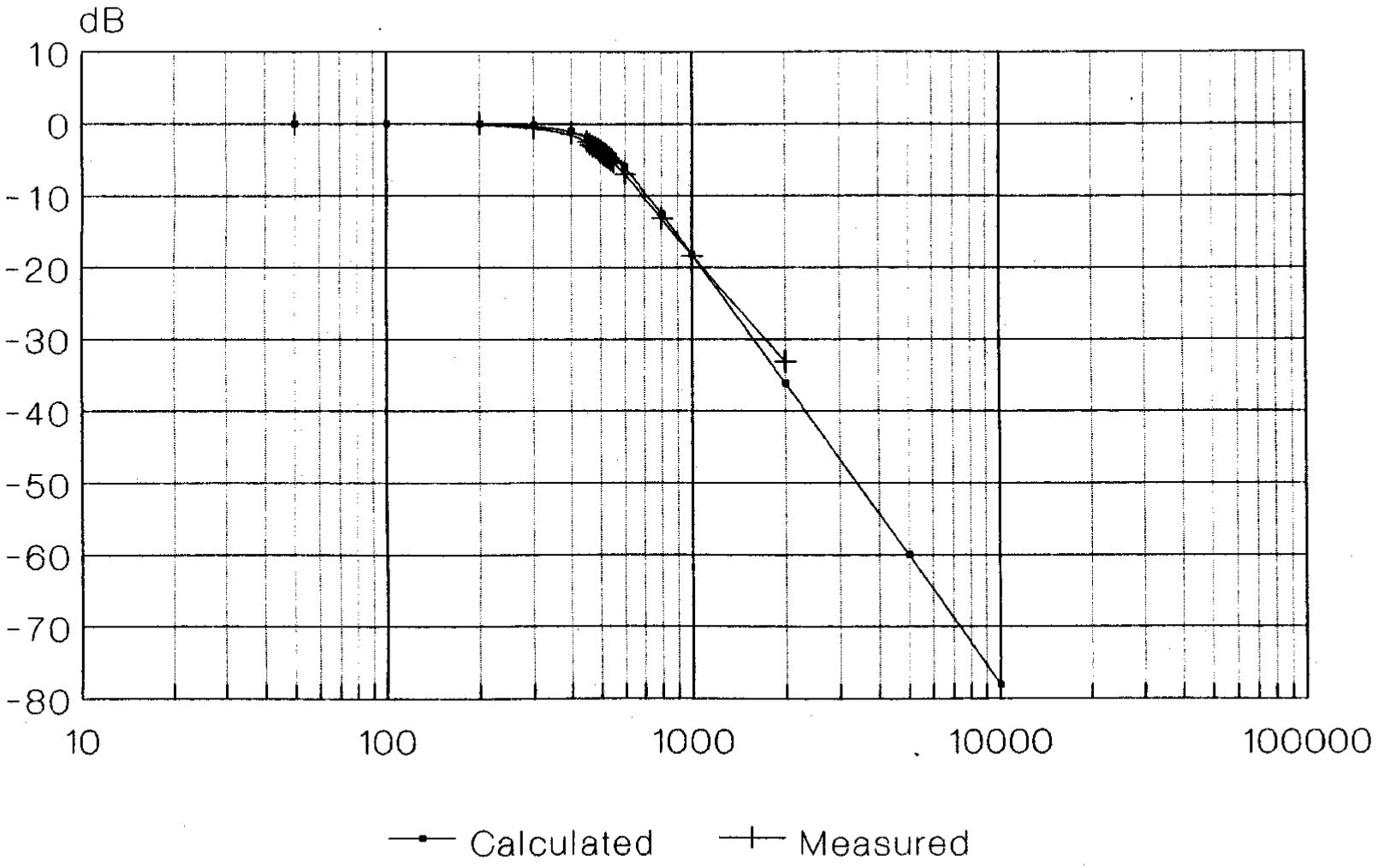
Graph 2. 7 kHz Low-pass Filter

Magnitude Response



Graph 3. 300-3000 Hz Bandpass Filter

Magnitude Response



Graph 4. 75 Hz Low-pass Filter

CONCLUSION

When the design of this technical report was commenced, a few important points had to be taken into account. When designing the delay circuit aliasing had to be into consideration when the heart of the delay circuit was being designed. If this delay circuit yielded any aliasing, the overall delayed output signal would not be as expected.

The point that had to be taken into account when the third-order filters were being designed was the coefficients of the transfer function. Meaning the second stage of the filter was required to have a certain value of z (dampening factor). In this case a dampening factor of 0.5 was used. A different dampening factor would be used if the filter was of a different order. This technical report contains all Butterworth filters.

When all the circuit diagrams of appendix A were constructed and put together, the overall goal of this technical report was achieved. The front speakers had a wide sound to them. The centre speakers consisted of only speech and the rear speakers consisted of a delayed sound. These pair of rear speakers sounded like they were really far away as compared to the other speakers. Hence "surround sound" was created.

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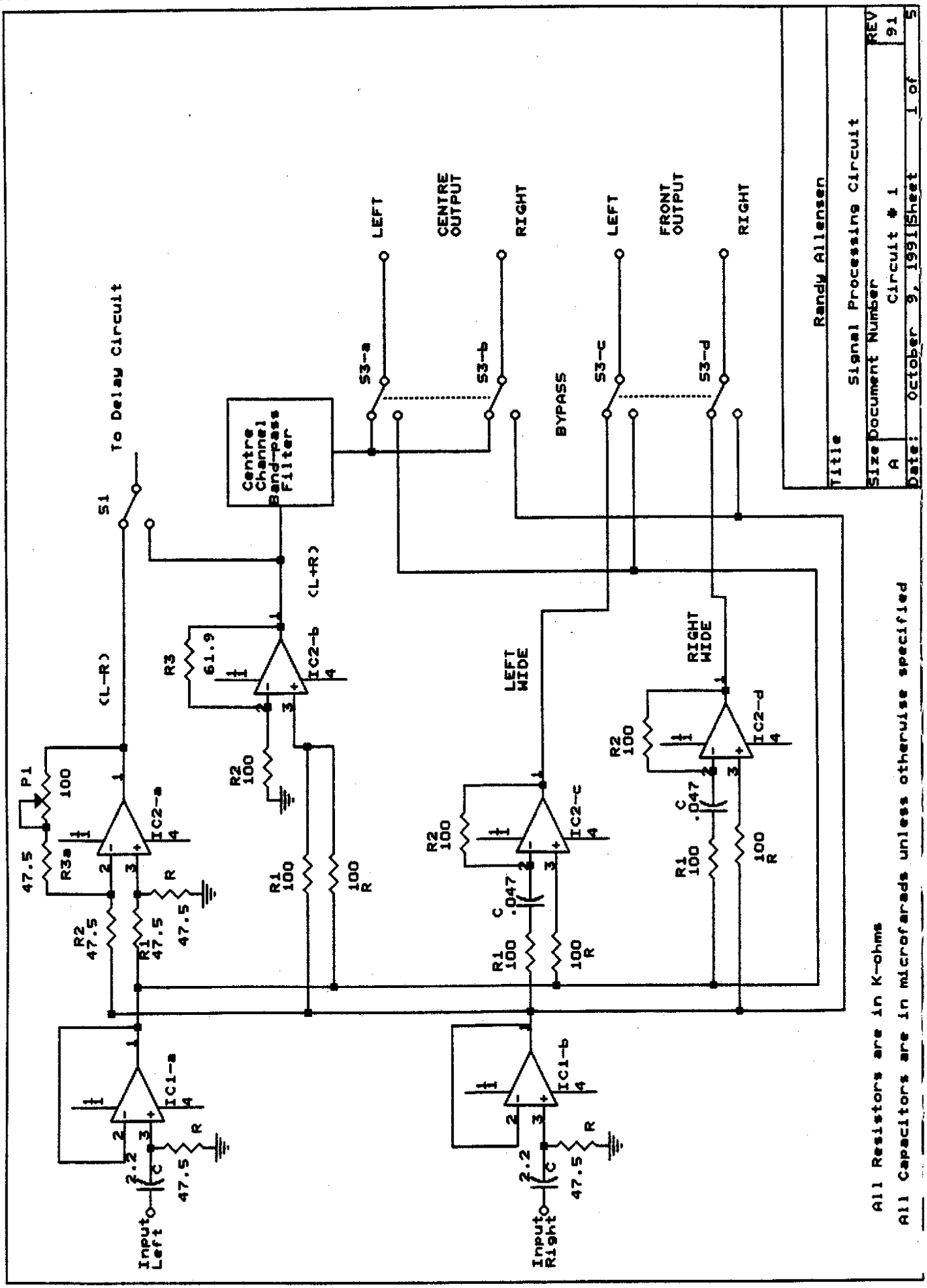
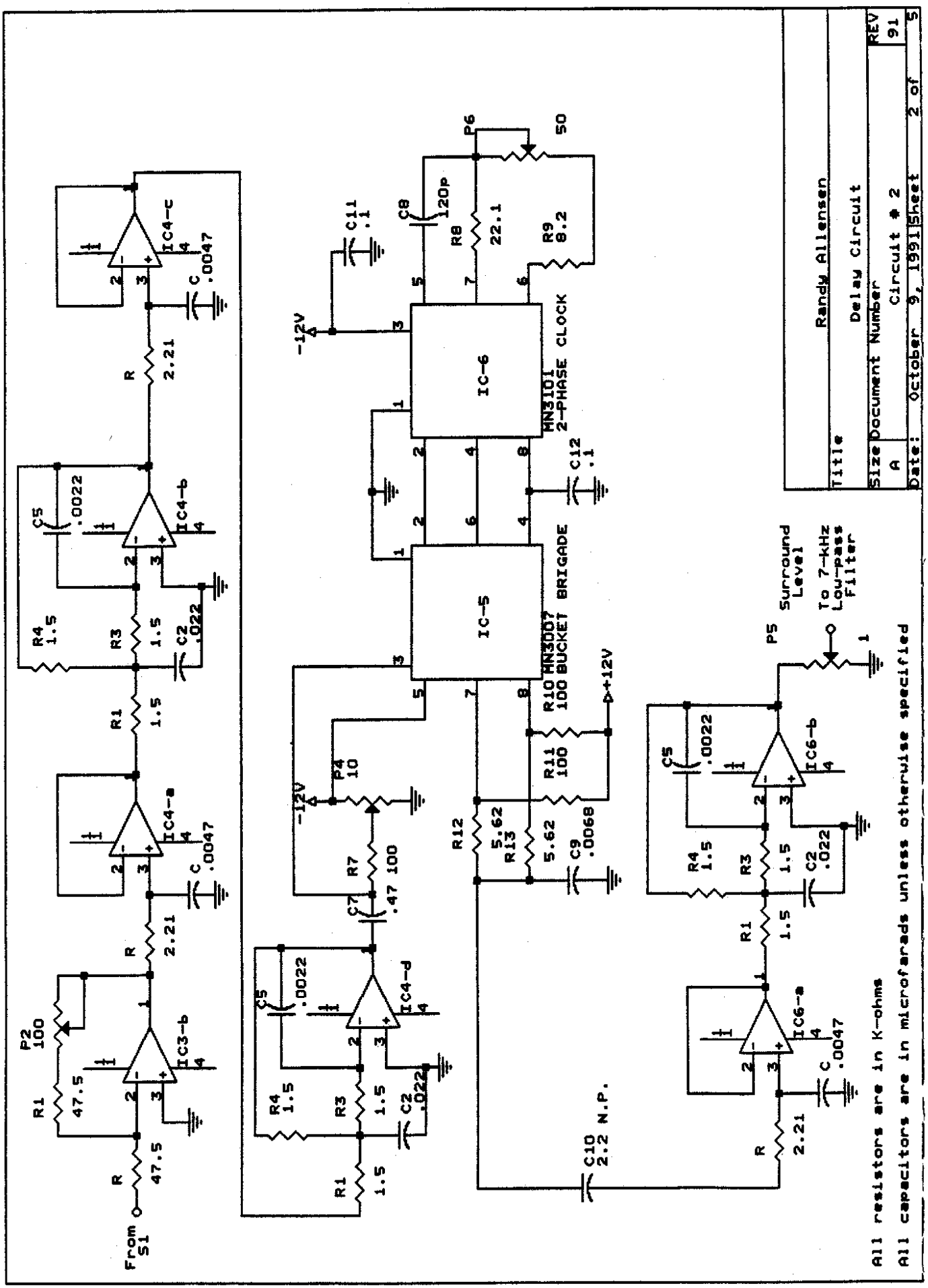
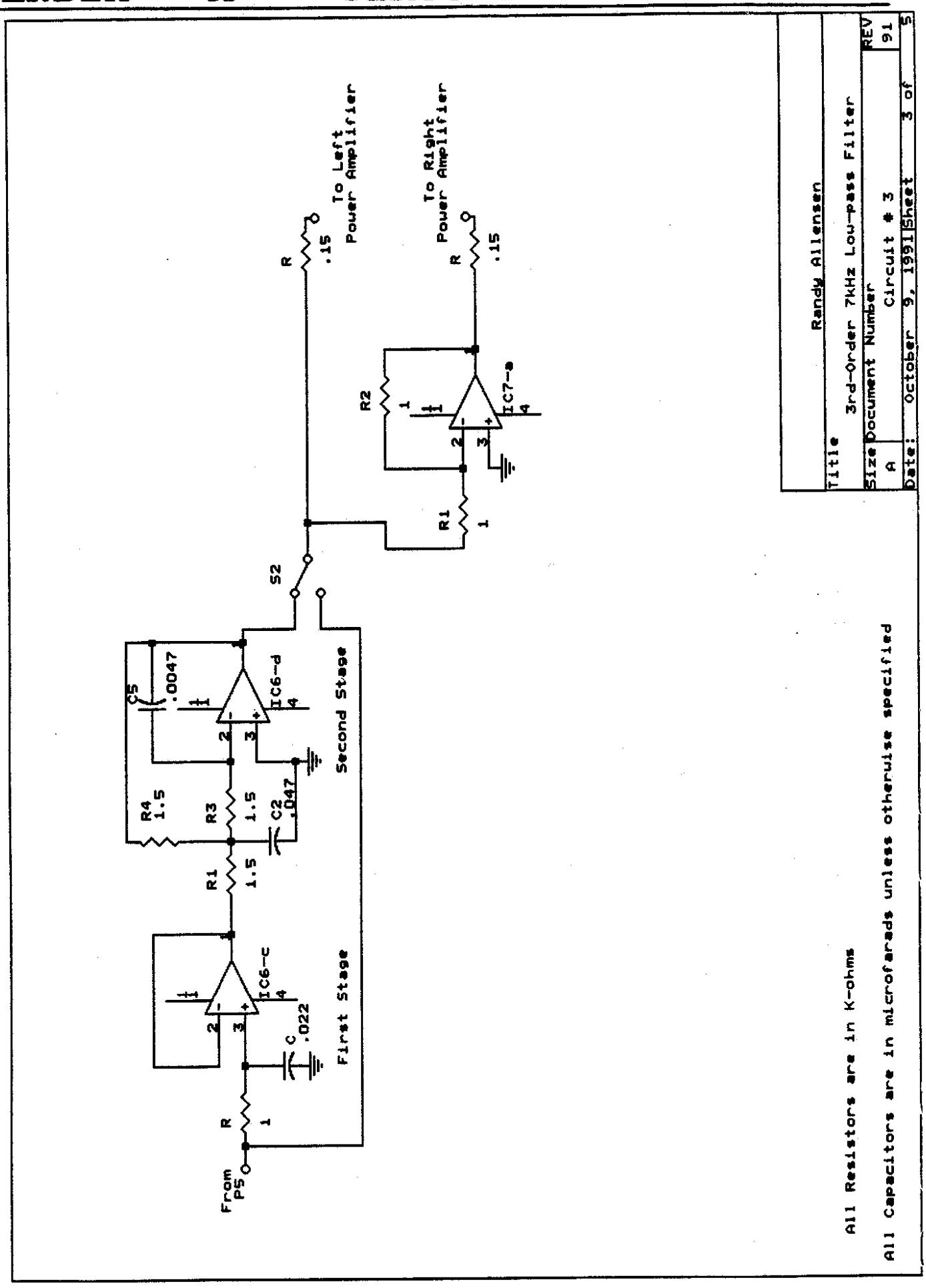
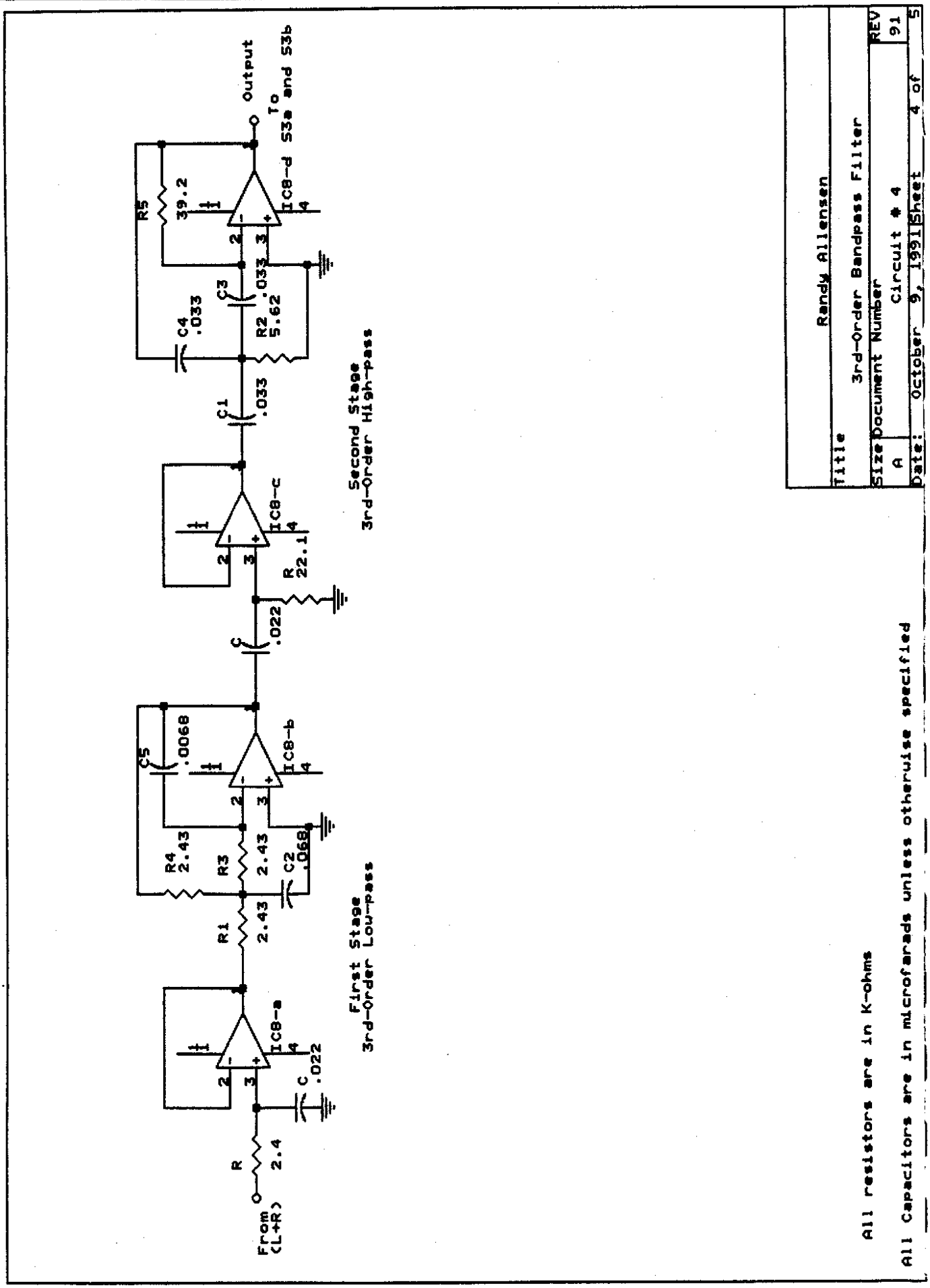
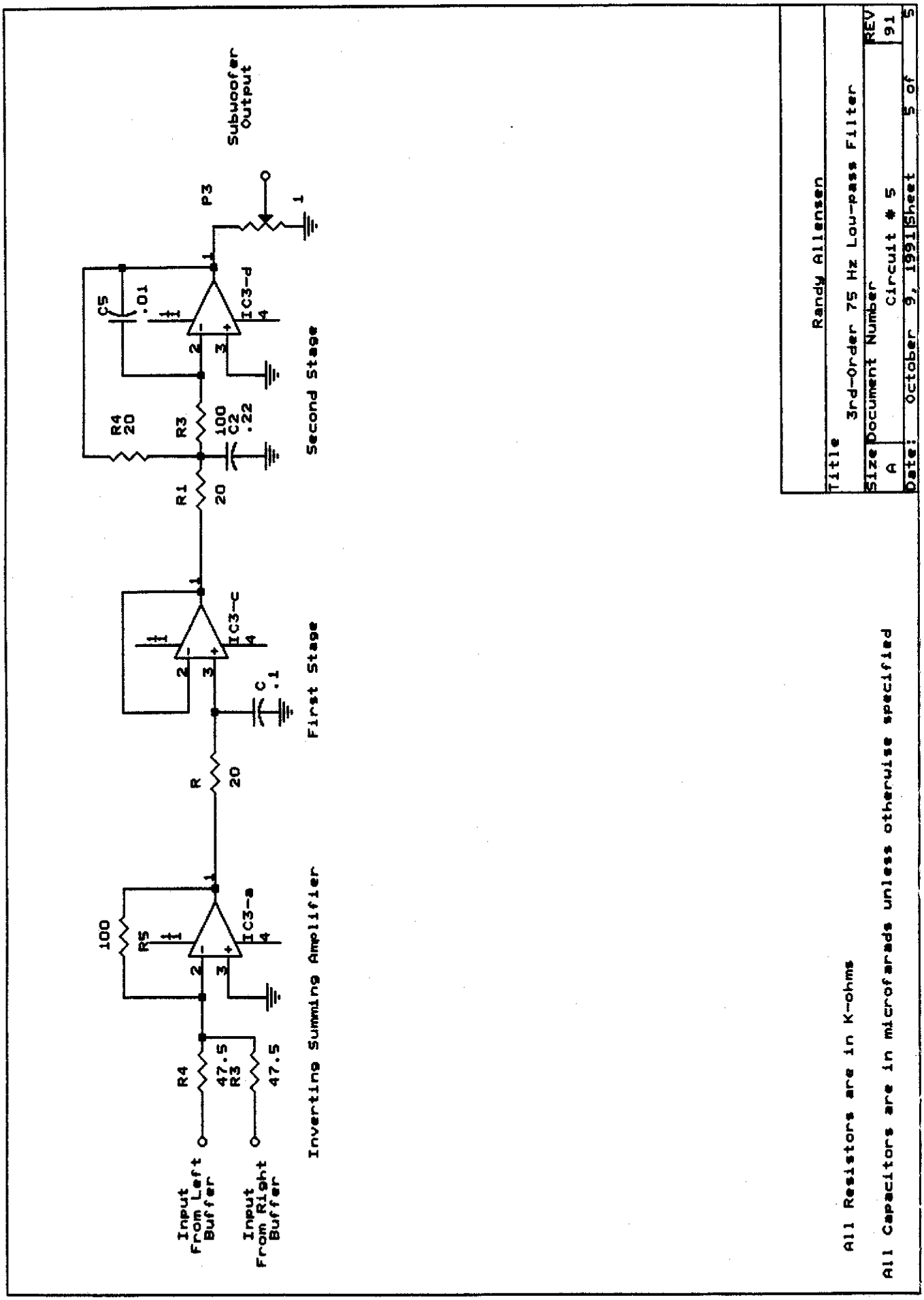

Randy Allensen
Title
Signal Processing Circuit
Size
A
Document Number
Circuit # 1
REV
91
Date: October 9, 1991 Sheet 1 of 5
All Resistors are in K-ohms
All Capacitors are in microfarads unless otherwise specified
To Delay Circuit
S1
Centre Channel Band-pass Filter
S3-a
S3-b
S3-c
S3-d
BYPASS
LEFT
CENTRE OUTPUT
RIGHT
LEFT
FRONT OUTPUT
RIGHT
(L-R)
(L+R)
LEFT WIDE
RIGHT WIDE
P1
100
47.5
R3a
IC2-a
IC2-b
IC2-c
IC2-d
IC1-a
IC1-b
R3
61.9
R2
100
R1
100
R
100
R2
47.5
R1
47.5
47.5
C
.047
2.2
47.5
Input Left
Input Right


Randy Allensen
Title
Delay Circuit
Size
A
Document Number
Circuit # 2
REV
91
Date: October 9, 1991 Sheet 2 of 5
All resistors are in K-ohms
All capacitors are in microfarads unless otherwise specified
From S1
P2 100
P4 10
P5
P6 50
Surround Level
To 7-kHz Low-pass Filter
IC3-b
IC4-a
IC4-b
IC4-c
IC4-d
IC5
IC6
MN3007 BUCKET BRIGADE
MN3101 2-PHASE CLOCK
IC6-a
IC6-b
C10 2.2 N.P.
R10 100
R11 100
R12 5.62
R13 5.62
C8 120P
C9 .0068
C11 .1
C12 .1
R1 47.5
R1 1.5
R2 2.21
R3 1.5
R4 1.5
R7 .47 100
R8 22.1
R9 8.2
C .0047
C2 .022
C5 .0022
+12V
-12V


To Left Power Amplifier
To Right Power Amplifier
R .15
R2
R1 1
IC7-a
S2
C5 .0047
IC6-d
R4 1.5
R3 1.5
C2 .047
R1 1.5
IC6-c
C .022
R 1
From PS
Second Stage
First Stage
Randy Allensen
Title 3rd-Order 7kHz Low-pass Filter
Size A
Document Number Circuit # 3
REV 91
Date: October 9, 1991 Sheet 3 of 5
All Resistors are in K-ohms
All Capacitors are in microfarads unless otherwise specified


Output To S3a and S3b
IC8-d
IC8-c
IC8-b
IC8-a
R5 39.2
C4 .033
C3 .033
R2 5.62
C1 .033
R 22.1
C .022
C5 .0068
R4 2.43
R3 2.43
C2 .068
R1 2.43
C .022
R 2.4
From (L+R)
Second Stage 3rd-Order High-pass
First Stage 3rd-Order Low-pass
Randy Allensen
Title 3rd-Order Bandpass Filter
Size A Document Number Circuit # 4 REV 91
Date: October 9, 1991 Sheet 4 of 5
All resistors are in K-ohms
All Capacitors are in microfarads unless otherwise specified


Subwoofer Output
P3
1
C5
.01
IC3-d
4
R4
20
R3
100
C2
.22
Second Stage
R1
20
IC3-c
C
.1
First Stage
R
20
100
R5
IC3-a
R4
47.5
R3
47.5
Input From Left Buffer
Input From Right Buffer
Inverting Summing Amplifier
Randy Allensen
Title
3rd-Order 75 Hz Low-pass Filter
Size
A
Document Number
Circuit # 5
REV
91
Date: October 9, 1991
Sheet
5 of
5
All Resistors are in K-ohms
All Capacitors are in microfarads unless otherwise specified

1. Signal Processing Circuit

The LF347N operational amplifier (used in each circuit).

IC1-a-b:

R = 47.5 kΩ metal film 1%
C = 2.2 μf 50V bi-polar radial electrolytic

IC2-a:

P1 = 100 kΩ (trimmer potentiometer - 20 turn)
R = R1 = R2 = R3a = 47.5 kΩ metal film 1%

IC2-b:

R3 = 61.9 kΩ metal film 2%
R = R1 = R2 =100 kΩ metal film 1%

IC2-c-d:

R = R1 = R2 = 100 kΩ
C = C = 0.047 μf metal polyester 5%

S1 = S3a = S3b = S3c = S3d = single pole, double throw

2. Delay Circuit

IC3-b:

P2 = 100 kΩ (trimmer potentiometer - 20 turn)
R = R1 = 47.5 kΩ metal film 1%

IC4-a:

R = 2.21 kΩ metal film 1%
C = 0.0047 µf metal film

IC4-b-d:

R1 = R3 = R4 = 1.5 kΩ metal film 1%
C2 = 0.022 µf metal film
C5 = 0.0022 µf metal film

IC4-c:

R = 2.21 kΩ metal film 1%
C = 0.0047 µf metal film

Delay:

C7 = 0.47 µf metal film
R7 = R10 = R11 = 100 kΩ metal film 1%
P4 = 10 kΩ (trimmer potentiometer - 20 turn)

IC-5 - MN3007 (1024 stage bucket brigade device - BBD)
IC-6 - MN3101 (2-phase clock frequency generator)
C8 = 120 pf ceramic disc 20%
R8 = 22.1 kΩ metal film 1%
R9 = 8.2 kΩ carbon film 5%
P6 = 50 kΩ (trimmer potentiometer - 20 turn)

R12 = R13 = 5.62 kΩ metal film 1%
C9 = 0.0068 µf axial monolithic 10%

2. Delay Circuit Continued

C10 = 2.2 μf 50V bipolar radial electrolytic
C11 = C12 = 0.1 μf metal film

IC6-a:

R = 2.21 kΩ metal film 1%
C = 0.0047 μf metal film

IC6-b:

R1 = R3 = R4 = 1.5 kΩ metal film 1%
C2 = 0.022 μf metal film
C5 = 0.0022 μf metal film

P5 = 1 kΩ (trimmer potentiometer - 20 turn)

3. Third-Order 7 kHz Low-pass Filter

IC6-c:

R = 1 kΩ metal film 1%
C = 0.022 μf metal film

IC6-d:

R1 = R3 = R4 = 1.5 kΩ metal film 1%
C2 = 0.047 μf metal film
C5 = 0.0047 μf metal film

IC7-a:

R1 = R2 = 1 kΩ metal film 1%
R = R = 150 Ω metal film 1%

S2 - single pole, double throw

4. Third-Order Bandpass Filter

IC8-a:

R = 2.4 kΩ carbon film 5%
C = 0.022 μf metal film

IC8-b:

R1 = R3 = R4 = 2.43 kΩ metal film 1%
C2 = 0.068 μf metal film
C5 = 0.0068 μf axial monolithic 10%

IC8-c:

R = 22.1 kΩ metal film 1%
C = 0.022 μf metal film

IC8-d:

R2 = 5.62 kΩ metal film 1%
R5 = 39.2 kΩ metal film 1%
C1 = C3 = C4 = 0.033 μf metal film

5. Third-Order 75 Hz Low-pass Filter

IC3-a:

R5 = 100 kΩ metal film 1%
R3 = R4 = 47.5 kΩ metal film 1%

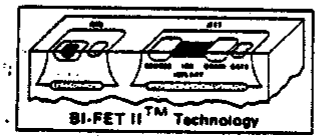
IC3-c:

R = 20 kΩ metal film 1%
C = 0.1 μf metal film

IC3-d:

R1 = R4 = 20 kΩ metal film 1%
R3 = 100 kΩ metal film %
C2 = 0.22 μf metal film
C5 = 0.01 μf metal film

National Semiconductor



LF147/LF347/LF347B Wide Bandwidth Quad JFET Input Operational Amplifiers

General Description

The LF147 is a low cost, high speed quad JFET input operational amplifier with an internally trimmed input offset voltage (BI-FET II™ technology). The device requires a low supply current and yet maintains a large gain bandwidth product and a fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The LF147 is pin compatible with the standard LM148. This feature allows designers to immediately upgrade the overall performance of existing LF148 and LM124 designs.

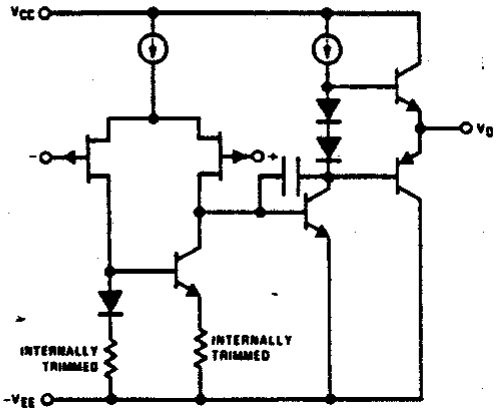
The LF147 may be used in applications such as high speed integrators, fast D/A converters, sample-and-hold circuits and many other circuits requiring low input offset voltage, low input bias current, high input impedance, high slew rate and wide bandwidth. The device has low noise and offset voltage drift.

Features

■ Internally trimmed offset voltage	5 mV max
■ Low input bias current	50 pA
■ Low input noise current	0.01 pA/$\sqrt{Hz}$
■ Wide gain bandwidth	4 MHz
■ High slew rate	13 V/μs
■ Low supply current	7.2 mA
■ High input impedance	$10^{12}\Omega$
■ Low total harmonic distortion $A_V = 10$, $R_L = 10k$, $V_O = 20$ Vp-p, BW = 20 Hz – 20 kHz	<0.02%
■ Low 1/f noise corner	50 Hz
■ Fast settling time to 0.01%	2 μs

Simplified Schematic

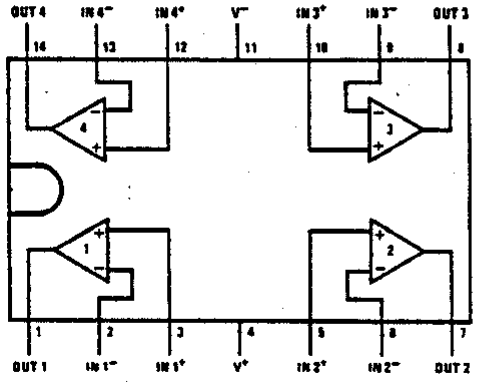
¼ Quad



TL/H/5647–13

Connection Diagram

Dual-In-Line Package



TL/H/5647–1

Top View

Order Number LF147D, LF347D, LF147J, LF347BJ, LF347J, LF347M, LF347WM, LF347BN or LF347N
See NS Package Number D14E, J14A, M14A, M14B or N14A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

	LF147	LF347B/LF347
Supply Voltage	±22V	±18V
Differential Input Voltage	±38V	±30V
Input Voltage Range (Note 1)	±19V	±15V
Output Short Circuit Duration (Note 2)	Continuous	Continuous
Power Dissipation (Notes 3 and 9)	900 mW	1000 mW
T_j max	150°C	150°C
θ_{jA}		
Cavity DIP (D) Package		80°C/W
Ceramic DIP (J) Package		70°C/W
Plastic DIP (N) Package		75°C/W
Surface Mount Narrow (M)		100°C/W
Surface Mount Wide (WM)		85°C/W

	LF147	LF347B/LF347
Operating Temperature Range	(Note 4)	(Note 4)
Storage Temperature Range	$-65°C \le T_A \le 150°C$	
Lead Temperature (Soldering, 10 sec.)	260°C	260°C
Soldering Information		
Dual-In-Line Package		
Soldering (10 seconds)		260°C
Small Outline Package		
Vapor Phase (60 seconds)		215°C
Infrared (15 seconds)		220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ESD rating to be determined.

DC Electrical Characteristics (Note 5)

Symbol	Parameter	Conditions	LF147			LF347B			LF347			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input Offset Voltage	$R_S = 10\ k\Omega$, $T_A = 25°C$ Over Temperature		1	5 8		3	5 7		5	10 13	mV mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	$R_S = 10\ k\Omega$		10			10			10		µV/°C
I_{OS}	Input Offset Current	$T_j = 25°C$, (Notes 5, 6) Over Temperature		25	100 25		25	100 4		25	100 4	pA nA
I_B	Input Bias Current	$T_j = 25°C$, (Notes 5, 6) Over Temperature		50	200 50		50	200 8		50	200 8	pA nA
R_{IN}	Input Resistance	$T_j = 25°C$		10^{12}			10^{12}			10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	$V_S = \pm 15V$, $T_A = 25°C$ $V_O = \pm 10V$, $R_L = 2\ k\Omega$ Over Temperature	50 25	100		50 25	100		25 15	100		V/mV V/mV
V_O	Output Voltage Swing	$V_S = \pm 15V$, $R_L = 10\ k\Omega$	±12	±13.5		±12	±13.5		±12	±13.5		V
V_{CM}	Input Common-Mode Voltage Range	$V_S = \pm 15V$	±11	+15 −12		±11	+15 −12		±11	+15 −12		V V
CMRR	Common-Mode Rejection Ratio	$R_S \le 10\ k\Omega$	80	100		80	100		70	100		dB
PSRR	Supply Voltage Rejection Ratio	(Note 7)	80	100		80	100		70	100		dB
I_S	Supply Current			7.2	11		7.2	11		7.2	11	mA

AC Electrical Characteristics (Note 5)

Symbol	Parameter	Conditions	LF147			LF347B			LF347			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
	Amplifier to Amplifier Coupling	$T_A = 25°C$, f = 1 Hz – 20 kHz (Input Referred)		−120			−120			−120		dB
SR	Slew Rate	$V_S = \pm 15V$, $T_A = 25°C$	8	13		8	13		8	13		V/μs
GBW	Gain-Bandwidth Product	$V_S = \pm 15V$, $T_A = 25°C$	2.2	4		2.2	4		2.2	4		MHz
e_n	Equivalent Input Noise Voltage	$T_A = 25°C$, $R_S = 100\Omega$, f = 1000 Hz		20			20			20		nV/$\sqrt{Hz}$
i_n	Equivalent Input Noise Current	$T_j = 25°C$, f = 1000 Hz		0.01			0.01			0.01		pA/$\sqrt{Hz}$

Note 1: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

Note 2: Any of the amplifier outputs can be shorted to ground indefinitely, however, more than one should not be simultaneously shorted as the maximum junction temperature will be exceeded.

Note 3: For operating at elevated temperature, these devices must be derated based on a thermal resistance of θ_{jA}.

Note 4: The LF147 is available in the military temperature range $-55°C \le T_A \le 125°C$, while the LF347B and the LF347 are available in the commercial temperature range $0°C \le T_A \le 70°C$. Junction temperature can rise to T_j max = 150°C.

Note 5: Unless otherwise specified the specifications apply over the full temperature range and for $V_S = \pm 20V$ for the LF147 and for $V_S = \pm 15V$ for the LF347B/LF347. V_{OS}, I_B, and I_{OS} are measured at $V_{CM} = 0$.

Note 6: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_j. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D. $T_j = T_A + \theta_{jA} P_D$ where θ_{jA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

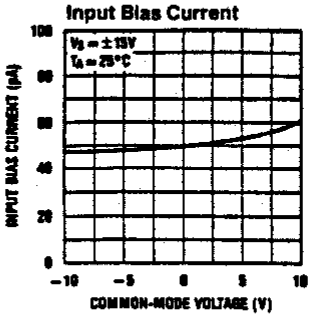
Note 7: Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice from $V_S = \pm 5V$ to $\pm 15V$ for the LF347 and LF347B and from $V_S = \pm 20V$ to $\pm 5V$ for the LF147.

Note 8: Refer to RETS147X for LF147D and LF147J military specifications.

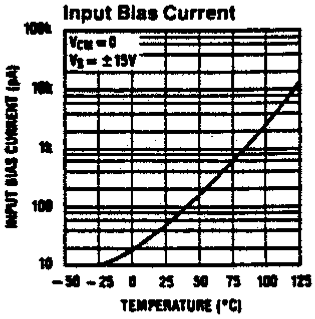
Note 9: Max. Power Dissipation is defined by the package characteristics. Operating the part near the Max. Power Dissipation may cause the part to operate outside guaranteed limits.

Typical Performance Characteristics

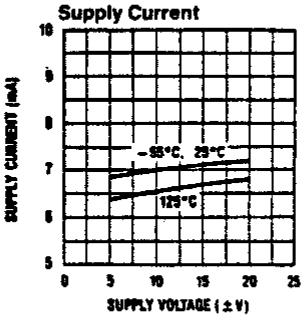
Input Bias Current



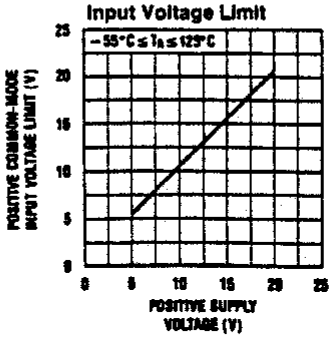
Input Bias Current



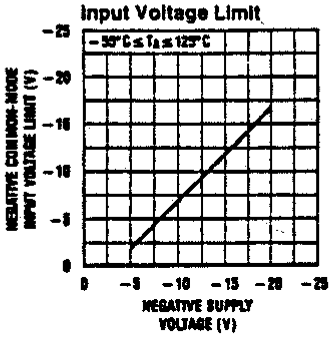
Supply Current



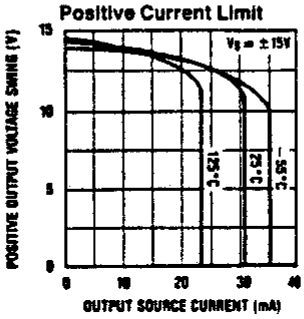
Positive Common-Mode Input Voltage Limit



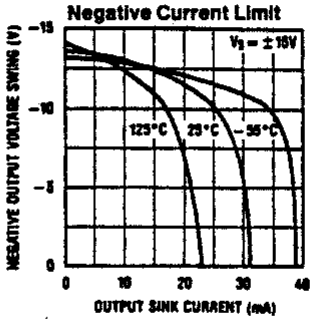
Negative Common-Mode Input Voltage Limit



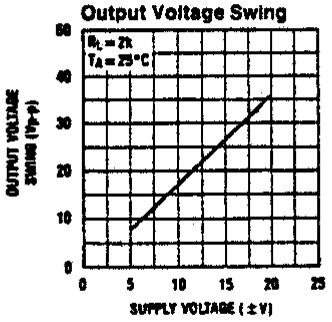
Positive Current Limit



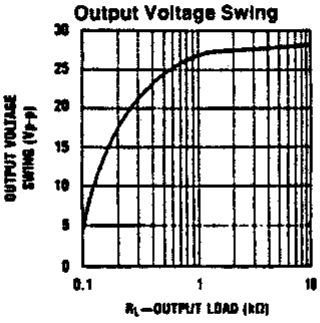
Negative Current Limit



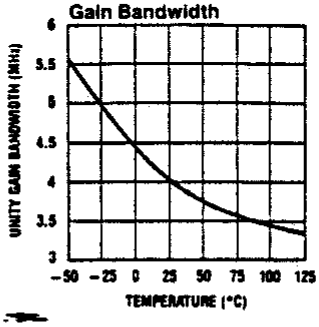
Output Voltage Swing



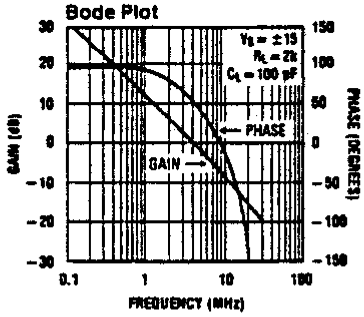
Output Voltage Swing



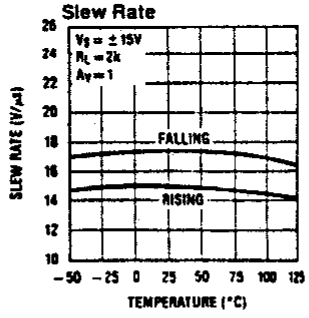
Gain Bandwidth



Bode Plot



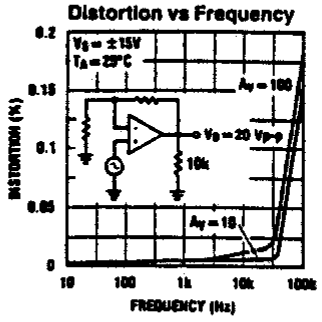
Slew Rate



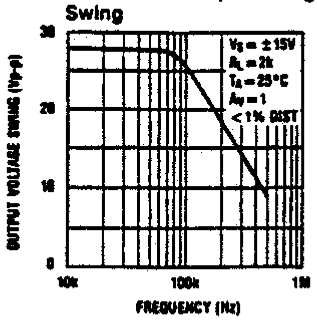
TL/H/5647-2

Typical Performance Characteristics (Continued)

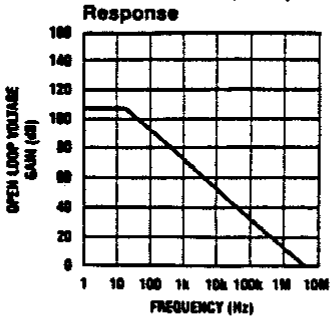
Distortion vs Frequency



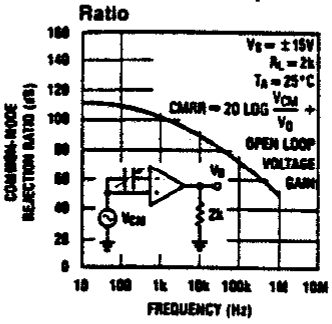
Undistorted Output Voltage Swing



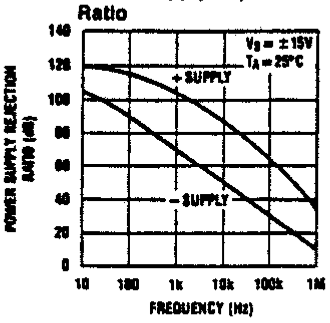
Open Loop Frequency Response



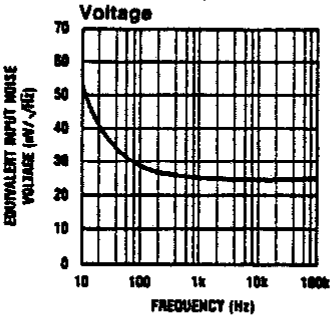
Common-Mode Rejection Ratio



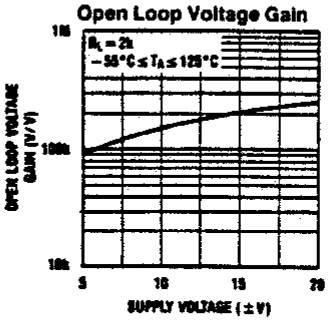
Power Supply Rejection Ratio



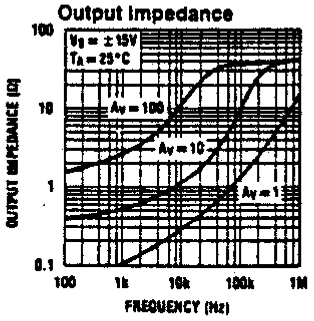
Equivalent Input Noise Voltage



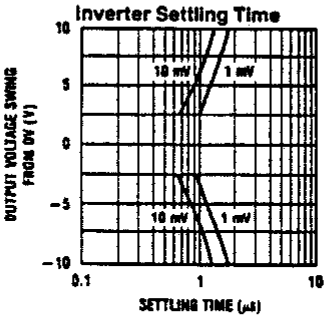
Open Loop Voltage Gain



Output Impedance



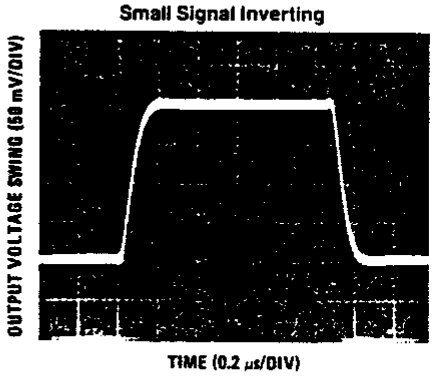
Inverter Settling Time



TL/H/5647–3

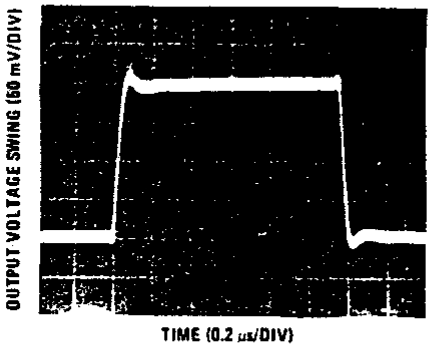
Pulse Response $R_L = 2\ k\Omega$, $C_L = 10\ pF$

Small Signal Inverting



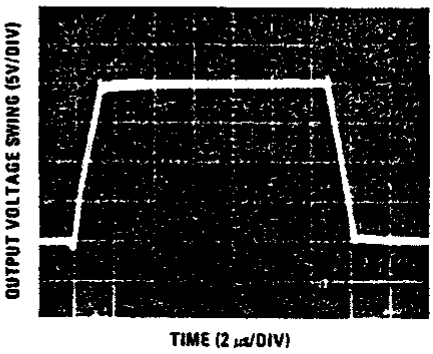
TL/H/5647–4

Small Signal Non-Inverting



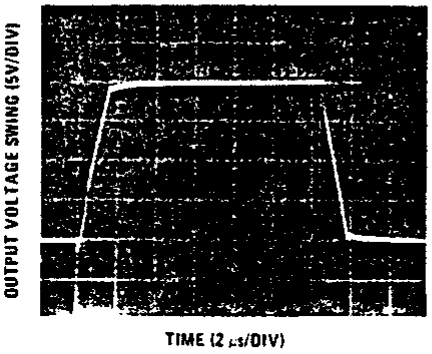
TL/H/5647–5

Large Signal Inverting



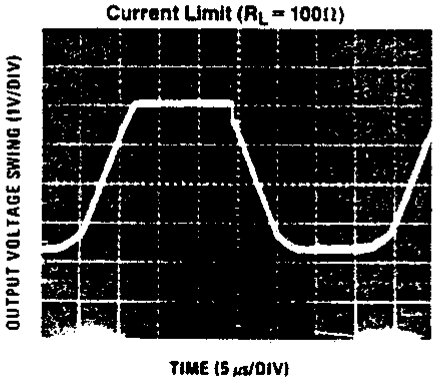
TL/H/5647–6

Large Signal Non-Inverting



TL/H/5647–7

Current Limit ($R_L = 100\Omega$)



TL/H/5647–8

Application Hints

The LF147 is an op amp with an internally trimmed input offset voltage and JFET input devices (BI-FET II™). These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will force the output to a high state, potentially causing a reversal of phase to the output. Exceeding the negative common-mode limit on both inputs will force the amplifier

Application Hints (Continued)

output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

The amplifiers will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

Each amplifier is individually biased by a zener reference which allows normal circuit operation on ±4.5V power supplies. Supply voltages less than these may result in lower gain bandwidth and slew rate.

The LF147 will drive a 2 kΩ load resistance to ±10V over the full temperature range. If the amplifier is forced to drive heavier load currents, however, an increase in input offset voltage may occur on the negative voltage swing and finally reach an active current limit on both positive and negative swings.

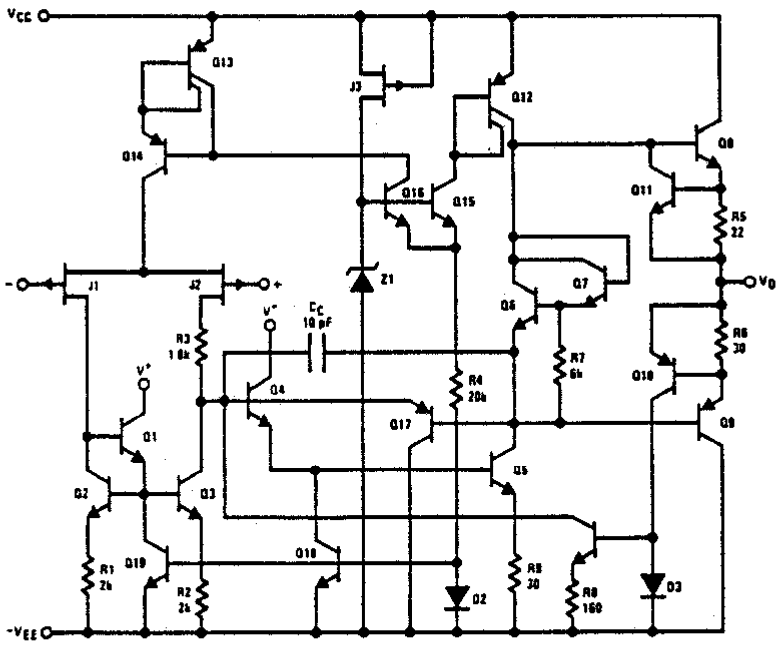
Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

Because these amplifiers are JFET rather than MOSFET input op amps they do not require special handling.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pick-up" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

Detailed Schematic



TL/H/5647-9

Clock Generator / Driver MN 3101 for BBD's

General Description

The MN3101 is a CMOS integrated circuit designed to generate low impedance two clock phases required for driving BBD's. In addition, the MN3101 provides the optimum V_{GG} for BBD's* when the MN3101 is used with BBD's on a common V_{DD} supply.

The self-contained oscillator can be controlled by an external RC circuit, but an external oscillator can also be used. The clock frequency is 1/2 of the oscillation frequency.

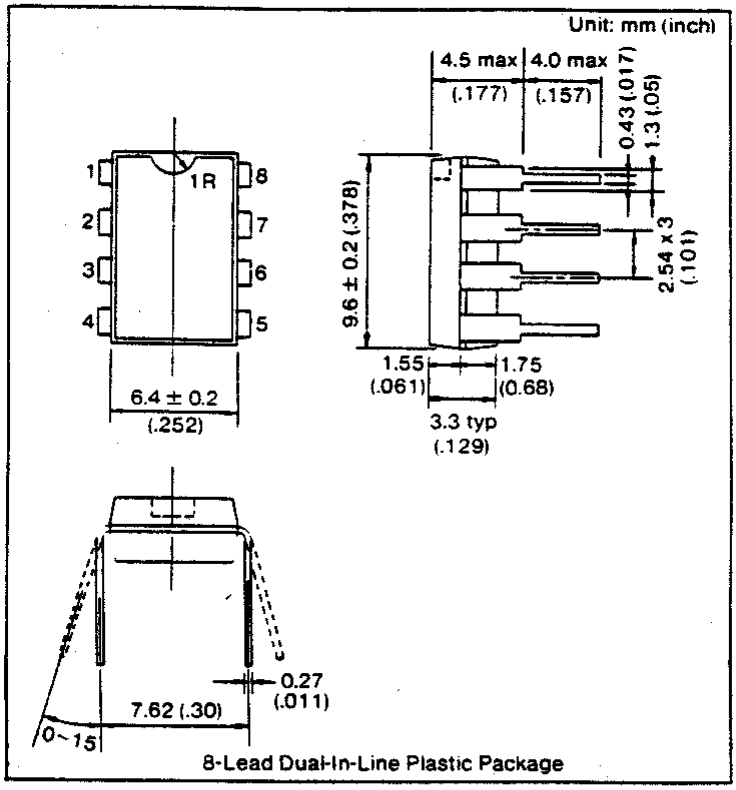
*PANASONIC's BBD product range: MN3001, MN3002, MN3003, MN3004, MN3005, MN3006, MN3007, MN3008, MN3009, MN3010, MN3011, MN3012. Note: The MN3003 is provided with an internal oscillator.

Features:

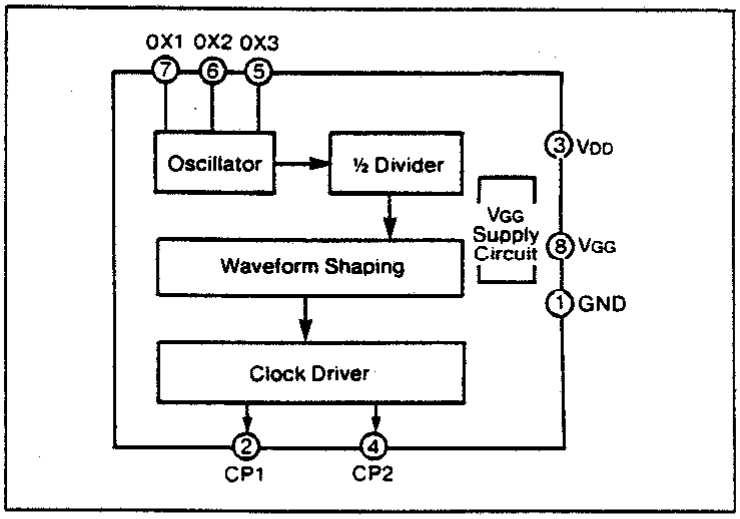
- **BBD direct driving capability – up to two MN3005 types (equivalent to 8192 stages).**
- **Either internal or external oscillator can be used**
- **Two phases (1/2 duty) output**
- **Provided with V_{GG} supply circuit**
- **Operates on a single power supply: – 8 ~ –16V**
- **8-lead dual-in-line plastic package**

Application

- **BBD clock generator/driver**



Block Diagram



Item	Symbol	Ratings	Unit
Supply Voltage	V_{DD}	−18~+0.3 *	V
Input Terminal Voltage	V_I	V_{DD} − 0.3~+0.3 *	V
Output Terminal Voltage	V_O	V_{DD} − 0.3~+0.3 *	V
Power Dissipation	P_D	200	mW
Operating Temperature	Topr	−10~+70	°C
Storage Temperature	Tstg	−30~+125	°C

*With respect to GND = OV.

Operating Conditions

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply Voltage	V_{DD}	GND = OV	−8	−15	−16	V

Electrical Characteristics (Ta = 25 °C, V_{DD} = −15V, GND = OV)

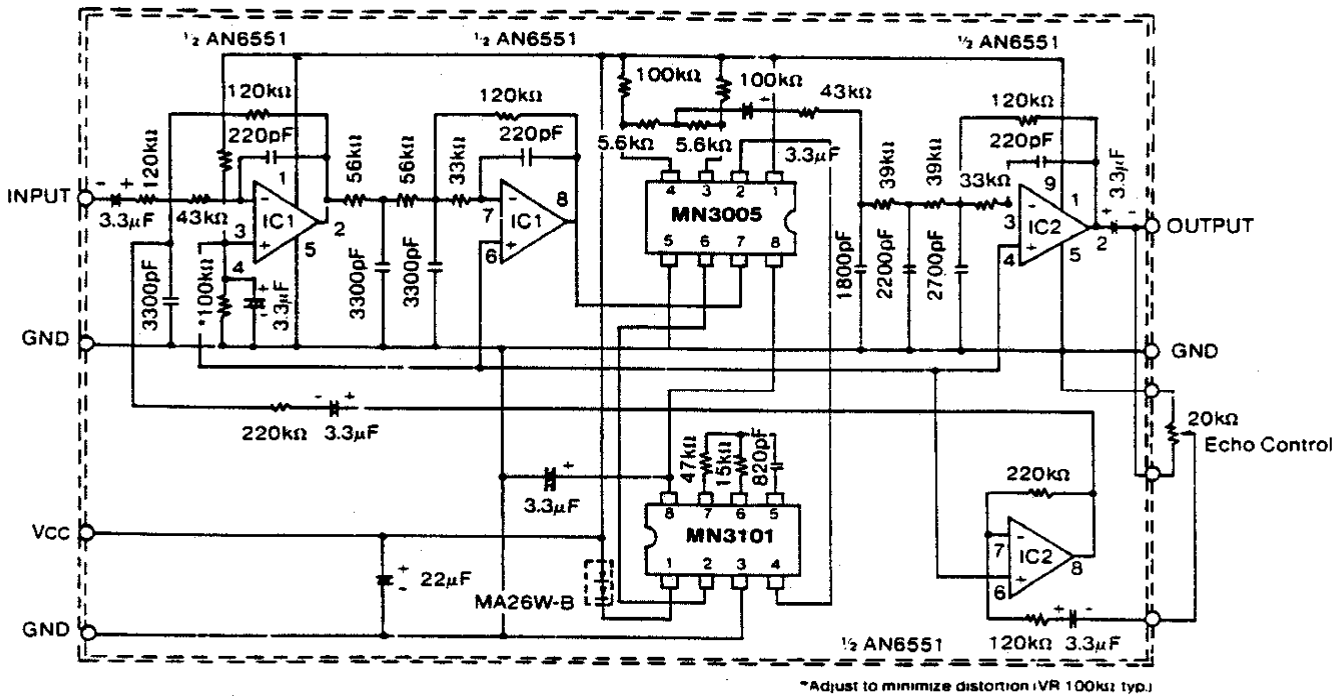
Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply Current	I_{DD}	Without load		3		mA
Power Consumption	Ptot	Clock output 40kHz		45		mW
OX1 Input Terminal						
Input Voltage "H" Level	V_{IH}		0		−1	V
Input Voltage "L" Level	V_{IL}		V_{DD}+1		V_{DD}	V
Input Leakage Current	I_{LK}	V_I = 0~−15V			30	μA
OX2 Output Terminal						
Output Current "H" Level	I_{OH1}	V_O = −1.0V	0.6			mA
Output Current "L" Level	I_{OL1}	V_O = −14V	0.5			mA
Output Leakage Current	I_{LOL1}	V_O = V_{DD}			30	μA
Output Leakage Current	I_{LOH1}	V_O = GND			30	μA
OX3 Output Terminal						
Output Current "H" Level	I_{OH2}	V_O = −1.0V	1.5			mA
Output Current "L" Level	I_{OL2}	V_O = −14V	2.0			mA
Output Leakage Current	I_{LOL2}	V_O = V_{DD}			30	μA
Output Leakage Current	I_{LOH2}	V_O = GND			30	μA
CP1, CP2 Output Terminal						
Output Current "H" Level	I_{OH3}	V_O = −1.0V	10			mA
Output Current "L" Level	I_{OL3}	V_O = −14V	10			mA
Output Leakage Current	I_{LOL3}	V_O = V_{DD}			30	μA
Output Leakage Current	I_{LOH3}	V_O = GND			30	μA
V_{GG} Output Terminal*						
Output Voltage	$V_{GG\ OUT}$			−14.0		V

*This terminal outputs VGG voltage particularly suitable for the BBD's manufactured by PANASONIC. The voltage is not necessarily suitable for the manufacturer's products.

The $V_{GG\ OUT}$ changes depending on V_{DD}. The relationship between $V_{GG\ OUT}$ and V_{DD} is as follows:

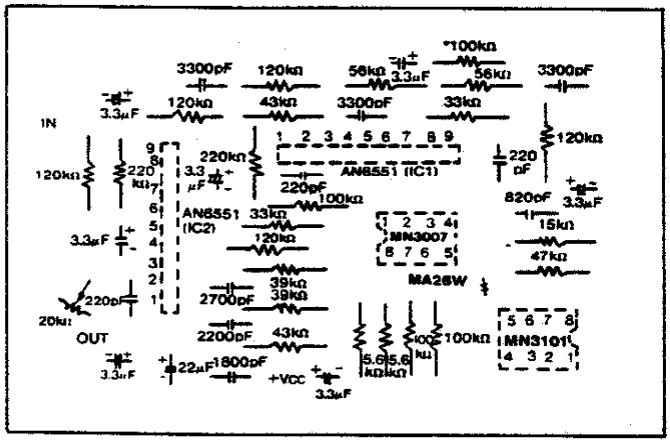
$V_{GG\ OUT}$ = 14/15 V_{DD}

Application Circuit Example 1 – Echo Effect Generation Circuit With The MN3005



*Adjust to minimize distortion (VR 100kΩ typ.)

Printed Circuit Board Layout (Actual Size)



Quick Reference Data for The MN3005

Item	Symbol	Value	Unit
Supply Voltage	VDD. VGG	−15. VDD +1	V
Signal Delay Time	tD	20.48 ~ 204.8	msec.
Total Harmonic Distortion	THD	1	%
Signal to Noise Ratio	S/N	75	dB

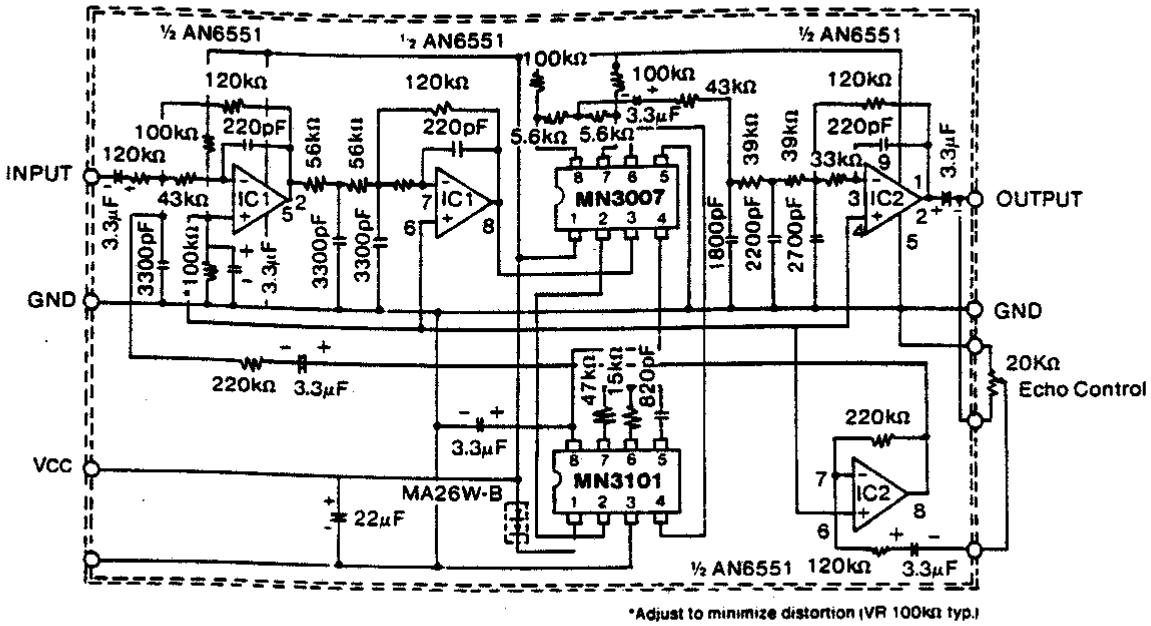
Quick Reference Data for the AN6551

Item	Symbol	Value	Unit
Supply Voltage	VCC	15	V
	VEE	−15	V
Input Bias Current	IB	500max.	nA
Voltage Gain	Gv	100typ.	dB
Noise Voltage Referred to Input	Vni	2.5typ.	μVrms
Maximum Output Voltage	Vo(max.)	±13typ.	V
Common-Mode Rejection Ratio	CMR	90typ.	dB
Supply Voltage Rejection	SVR	30typ.	μV/V

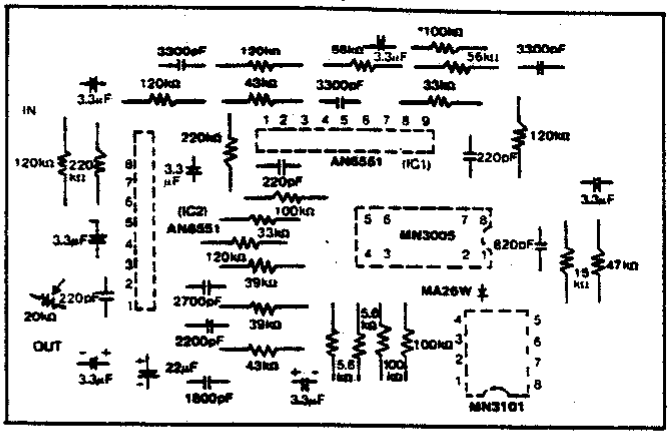
Electrical Characteristics of The Application Circuit Using The MN3005 (Vcc = 9V. Ta = 25 C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply Current	ICC			8	10	mA
Total Power Consumption	Ptot			70		mW
Signal Delay Time	tD	fcp = 18±2kHz	100	113	128	msec
Cutoff Frequency	fco			2		kHz
Input Signal Swing	Vi	THD = 2.5%			500	mVrms
Insertion Loss	Li	fi = 1kHz. Vi = 300mV	−2	0	2	dB
Total Harmonic Distortion	THD	Fi = 1kHz. Vi = Vi(max.) −6dB		0.5	1	%
Output Noise Voltage	Vno	Vi = OV			0.35	mVrms
Signal to Noise Ratio	S/N	Vi: Vi(max.) = 500mVrms				

Application Circuit Example 2 – Echo Effect Generation Circuit With The MN3007



Printed Circuit Board Layout (Actual Size)



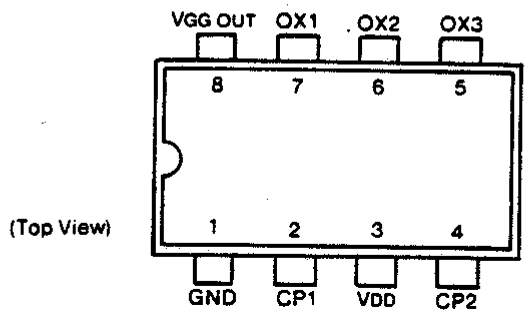
Quick Reference Data for The MN3007

Item	Symbol	Value	Unit
Supply Voltage	VDD. VGG	−15, V_{DD} +1	V
Signal Delay Time	tD	5.12 ~ 51.2	msec.
Total Harmonic Distortion	THD	0.3	%
Signal to Noise Ratio	S/N	88	dB

Electrical Characteristics of The Application Circuit Using The MN3007 (Vcc = 9V, Ta = 25 C)

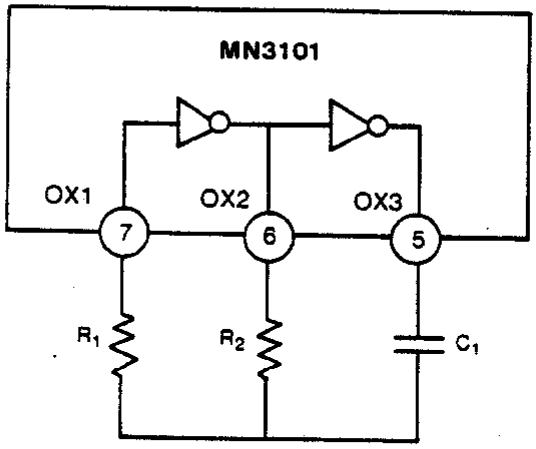
Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply Current	ICC			8	10	mA
Total Power Consumption	Ptot			70		mW
Signal Delay Time	tD	fcp = 14±2kHz	32	37	43	msec
Cutoff Frequency	fco			2		kHz
Input Signal Swing	Vi	THD = 2.5%			500	mVrms
Insertion Loss	Li	fi = 1kHz, Vi = 300mV	−2	0	2	dB
Total Harmonic Distortion	THD	fi = 1kHz, Vi = Vi(max.) −6dB		0.5	1	%
Output Noise Voltage	Vno	Vi = OV			0.35	mVrms
Signal to Noise Ratio	S/N	Vs Vi(max.) = 500mVrms	60			dB

Terminal Assignments



Pin No.	Symbol	I/O	Functions	
1	GND	Supply	Grounding	
2	CP1	O	Outputs 1/2 duty cycle clock pulse at frequency 1/2 of an oscillation frequency, having an opposite phase relationship with respect to CP2.	
3	V_{DD}	Supply	−15V supply voltage input.	
4	CP2	O	Outputs clock pulse having an opposite phase relationship with respect to CP1.	
5	OX3	O	Internal Oscillation:	External Oscillation:
6	OX2	O	C R network connection to the pins	An external oscillation input to OX1.
7	OX1	I	(See oscillator circuit example)	with OX2 and OX3 open.
8	$V_{GG\ OUT}$	O	−14V output (When V_{DD} = 15V) The relationship between V_{DD} and $V_{GG\ OUT}$ is: V_{GG} OUT = 14/15 V_{DD}	

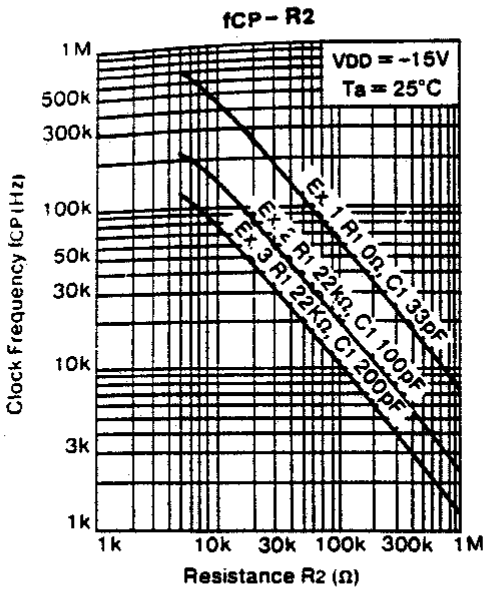
Oscillator Circuit Example

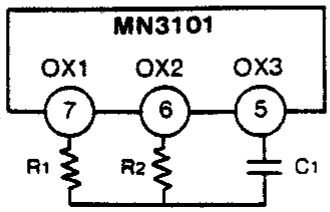


The internal oscillation circuit of the MN3101 consists of a 2-stage inverter. The oscillation frequency is established by the time constant of C_1 and R_2. The following table shows examples of C_1, R_1 and R_2 values. Fcp – R_2 characteristics example is shown in Figure 1.

Example \ Constant	R1 (Ω)	R2 (Ω)	C1 (pF)	f osc** (kHz)	F CP* (kHz)
Example 1	0	5k~1M	33	15~1500	7.5~750
Example 2	22k	5k~1M	100	5.2~440	2.6~220
Example 3	22k	5k~1M	200	1.4~280	0.7~140

*Clock output frequency for CP1 or CP2.
**Oscillation frequency for OX1, OX2, and OX3.





Maximum Clock Frequency

The maximum clock frequency is limited by device power dissipation and load capacitance. The power consumption of the devices increases as the clock frequency or load capacitance is increased (See Fig. 2). Therefore, a proper clock frequency and load capacitance value must be chosen so that the maximum allowable power dissipation of 200mW for the MN3101 is not exceeded.

Fig. 3 shows the relationship between the maximum frequency and load capacitance for 150mW power dissipation. The maximum clock frequency can be increased without increasing the power consumption when a resistor is connected to each clock output terminal (See Fig. 2 and 3). The series resistor consumes a part of the power required for driving the load capacitance and help reduce the power dissipated in the device.

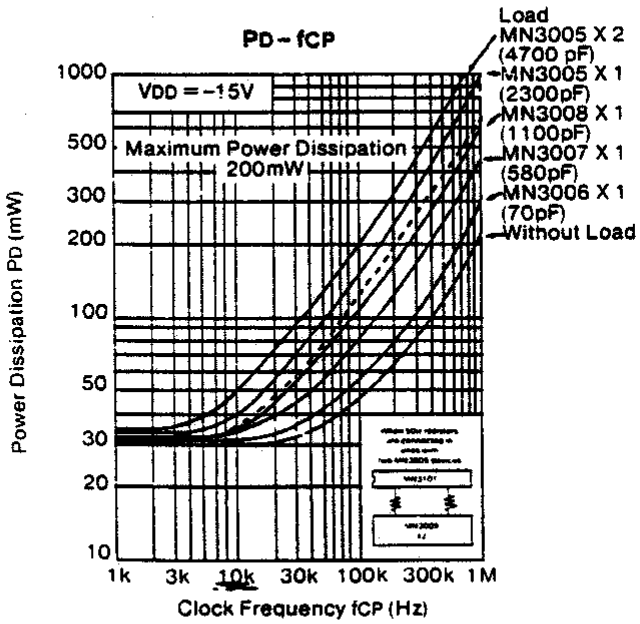


Fig. 2 Power Consumption vs Clock Frequency

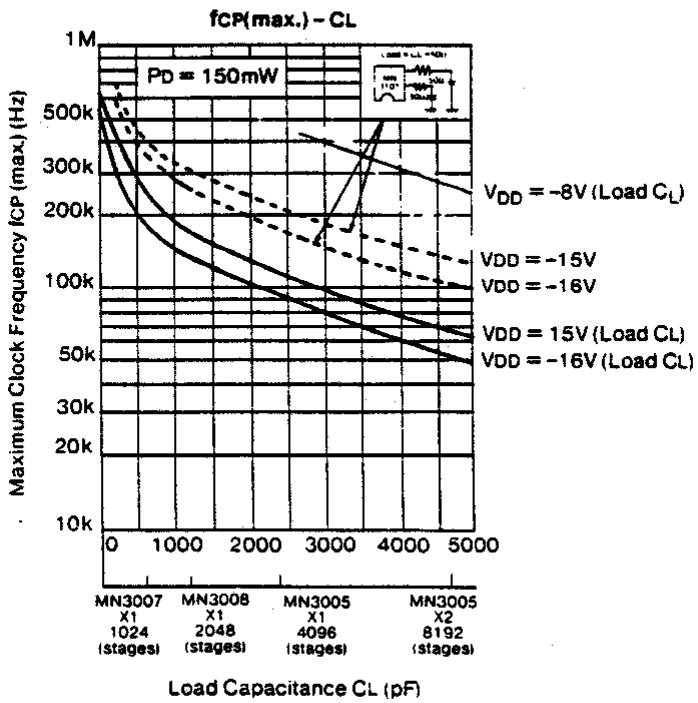


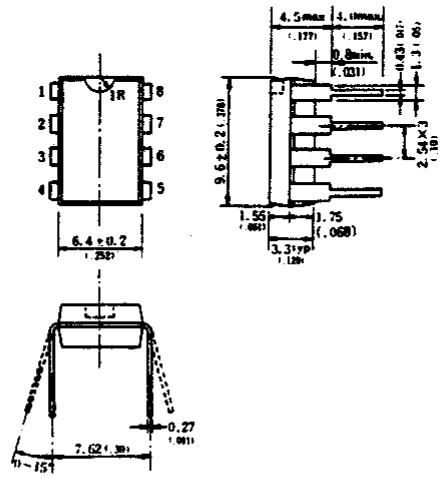
Fig. 3 Maximum Clock Frequency vs Load Capacitance at 150mW Power Consumption

1024-STAGE LOW NOISE BBD

General Description

The MN3007 is a 1024-stage long delay BBD (Bucket Brigade Device) that provides a signal delay of up to 51.2msec. The MN3007 is particularly suitable for use as variable signal delay lines in audio frequency range.

Unit : mm (inch)



8-Lead Dual-In-Line Plastic Package

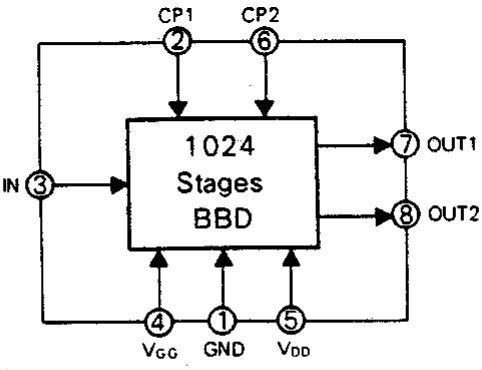
Features:

- **Wide range of variable delay time: 5.12~51.2msec.**
- **Clock component cancellation capability.**
- **No insertion loss: $L_i \simeq 0$ dB typ.**
- **Wide dynamic range: S/N ≃ 80 dB typ.**
- **Wide frequency response: $f_i < 12$kHz.**
- **Total harmonic distortion: THD=0.5% typ. (V_i=0.78Vrms)**
- **Clock frequency range: 10~100kHz.**
- **P-channel silicon gate, tetrode MOS transistors configuration**
- **8-lead dual-in-line plastic package.**

Applications:

- **Reverberation effect of echo microphones and stereo equipment.**
- **Chorus effects in electronic musical instruments.**
- **Variable or fixed delay of analog signals.**

Block Diagram



Quick Reference Data

Item	Symbol	Value	Unit
Supply Voltage	V_{DD}, V_{GG}	15, V_{DD} - 1	V
Signal Delay Time	t_D	5.12, 51.2	msec
Total Harmonic Distortion	THD	0.5	%
Signal to Noise Ratio	S/N	80	dB

Absolute Maximum Ratings (Ta=25℃)

Item	Symbol	Ratings	Unit
Terminal Voltage	V_{DD}, V_{GG}, V_{CP}, V_I	−18～+0.3	V
Output Voltage	V_O	−18～+0.3	V
Operating Temperature	Topr	−20～+60	℃
Storage Temperature	Tstg	−55～+125	℃

Operating Conditions (Ta=25℃)

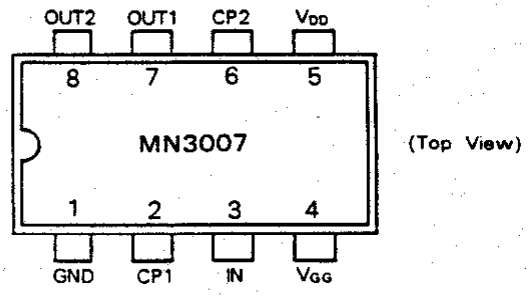
Item	Symbol	Min.	Typ.	Max.	Unit
Drain Supply Voltage	V_{DD}	−14	−15	−16	V
Gate Supply Voltage	V_{GG}		V_{DD}+1		V
Clock Voltage "H" Level	V_{CPH}	0		−1	V
Clock Voltage "L" Level	V_{CPL}		V_{DD}		V
Clock Input Capacitance	C_{CP}			700	pF
Clock Frequency	f_{CP}	10		100	kHz
Clock Pulse Width *2	t_{cpw}			0.5T *1	
Clock Rise Time *2	t_{cpr}			500	nsec
Clock Fall Time *2	t_{cpf}			500	nsec
Clock Cross Point	Vx	0		−3	V

*1 $T=1/f_{CP}$ *2 Clock Pulse Waveforms

Electrical Characteristics (Ta=25℃, $V_{DD}=V_{CPL}=-15V$, $V_{CPH}=0V$, $V_{GG}=-14V$, $R_L=100k\Omega$)

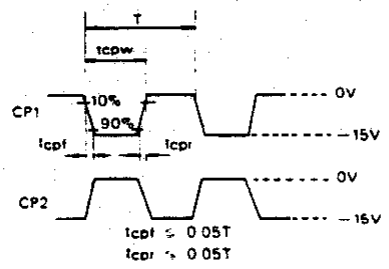
Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Signal Delay Time	t_D		5.12		51.2	msec
Input Signal Frequency	f_i	f_{cp}=40kHz, V_i=1.5Vrms, 3dB down (0dB at f_i=1kHz)			12	kHz
Input Signal Swing	V_i	f_{cp}=40kHz, f_i=1kHz, THD=2.5%			1.5	Vrms
Insertion Loss	L_i	f_{cp}=40kHz, f_i=1kHz, V_i=1.5Vrms	−4	0	4	dB
Total Harmonic Distortion	THD	f_{cp}=40kHz, f_i=1kHz, V_i=0.78Vrms		0.5	2.5	%
Noise Voltage	Vno	f_{cp}=100kHz Weighted by "A" curve			0.30	mVrms
Signal to Noise Ratio	S/N			80		dB

Terminal Assignments

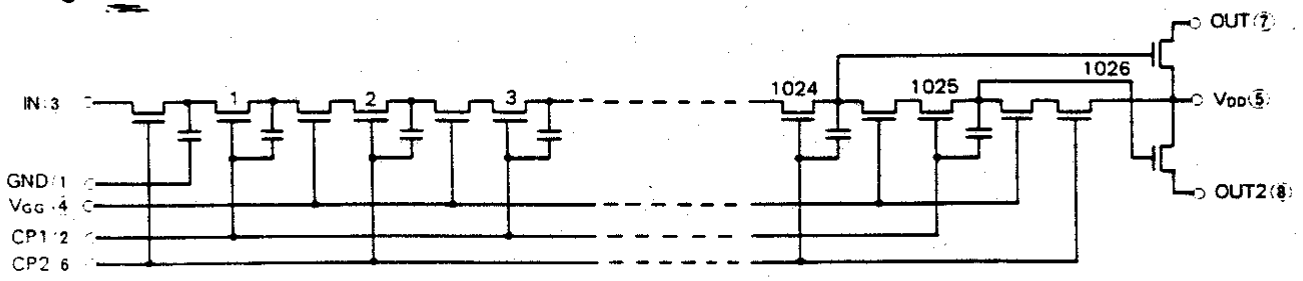


(Top View)

Clock Pulse Waveforms

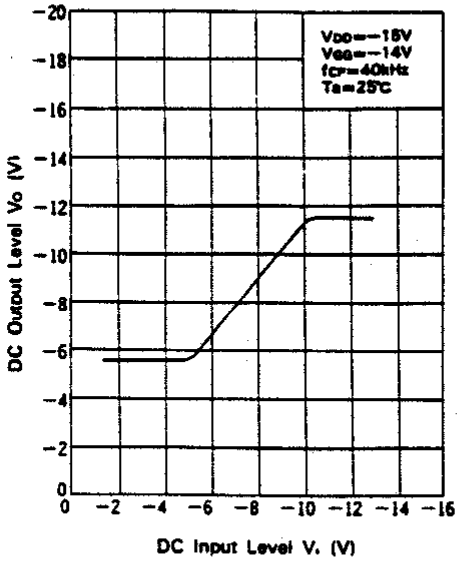


Circuit Diagram

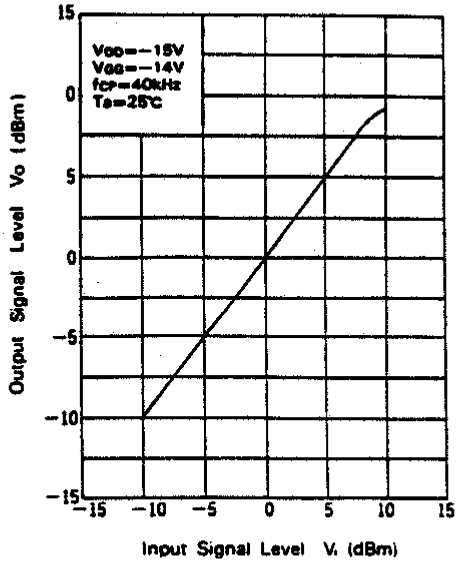


Typical Electrical Characteristic Curves

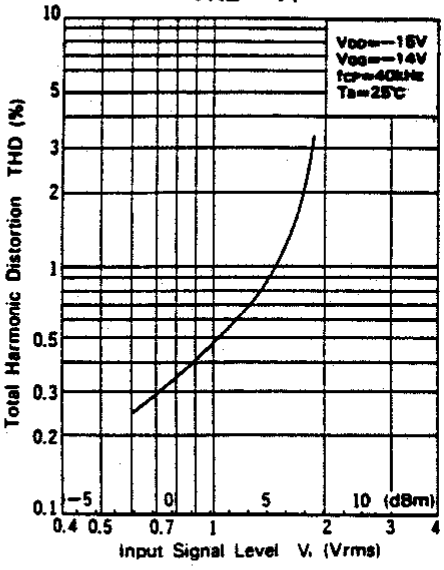
Vo—VI



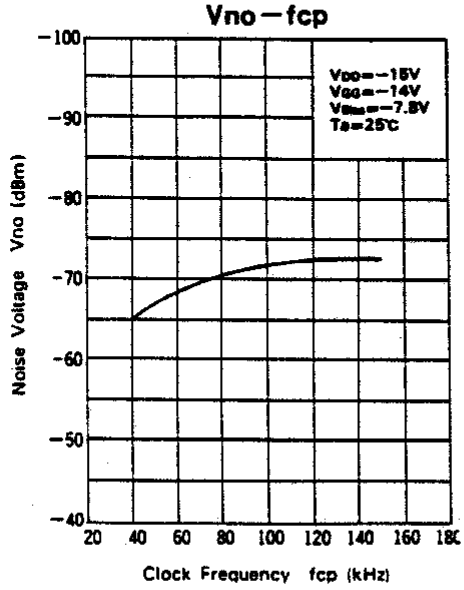
Vo—Vi



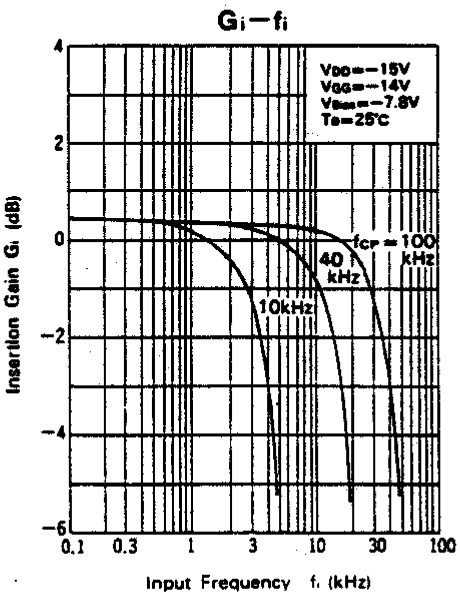
THD—Vi



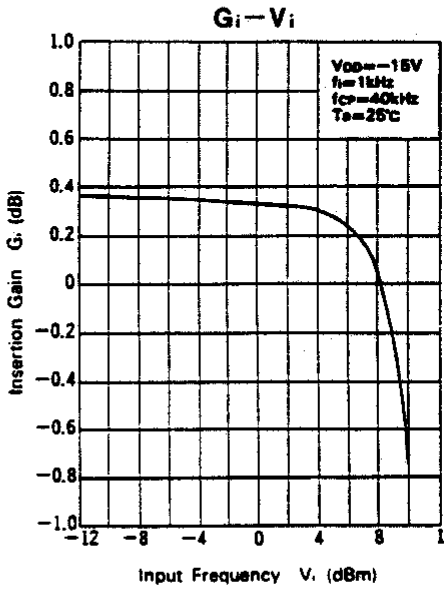
Vno—fcp



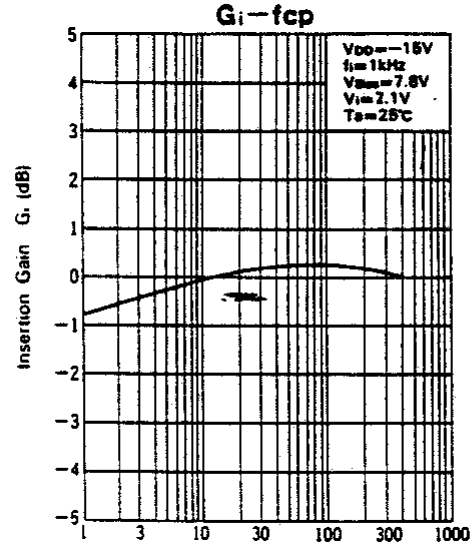
Gi—fi



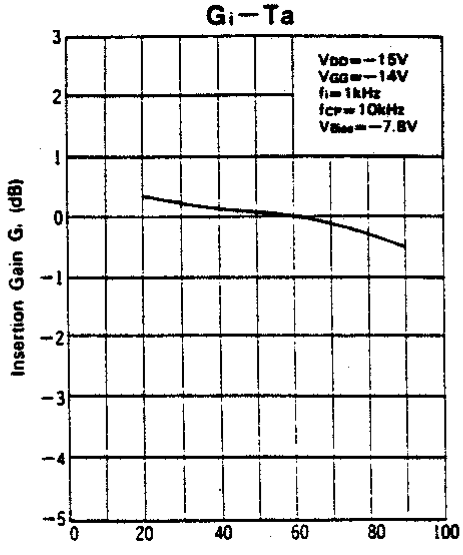
Gi—Vi



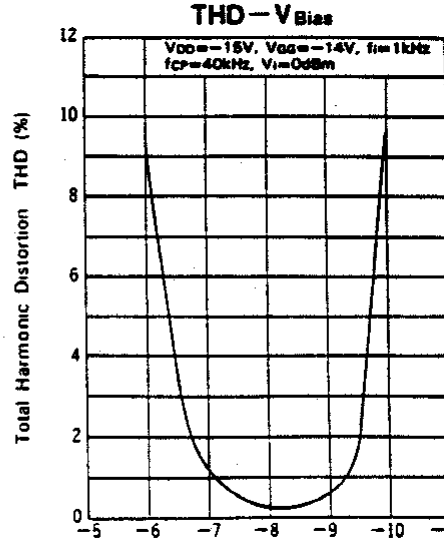
Gi—fcp



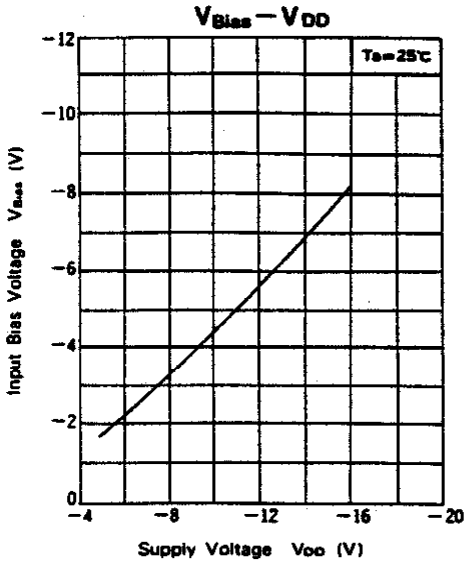
Gi—Ta

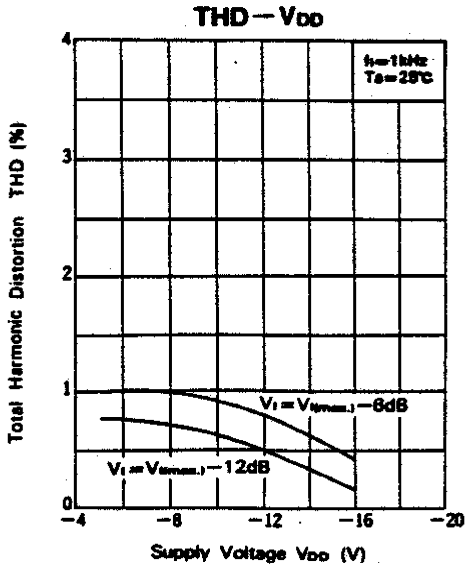


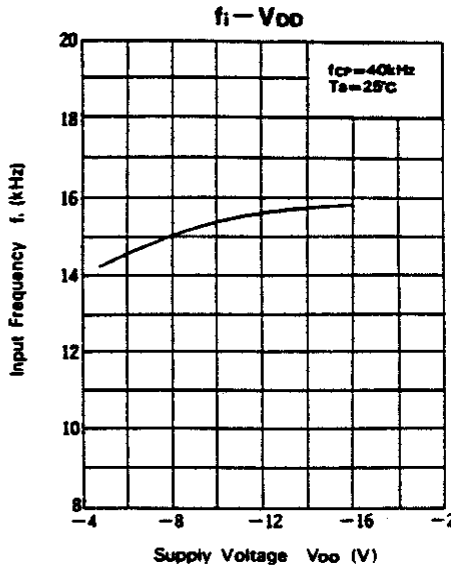
THD—VBias

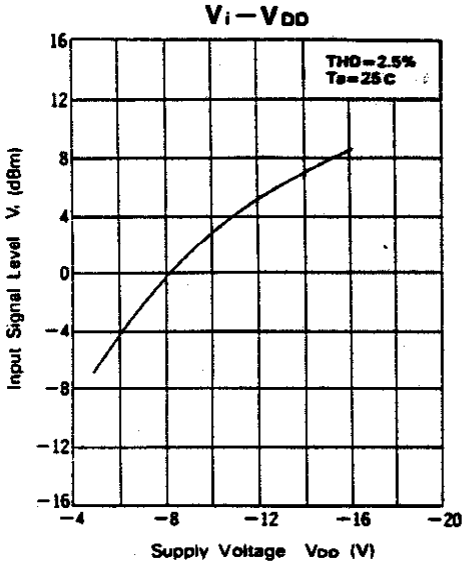


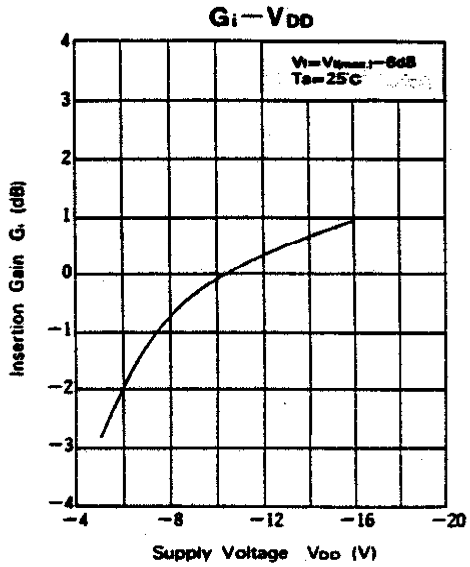
Supply Voltage Characteristics

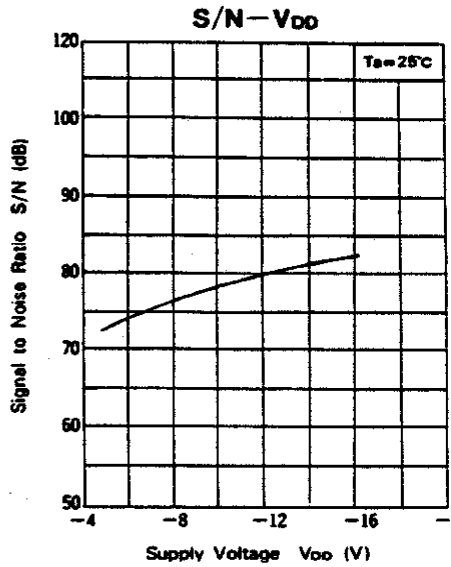




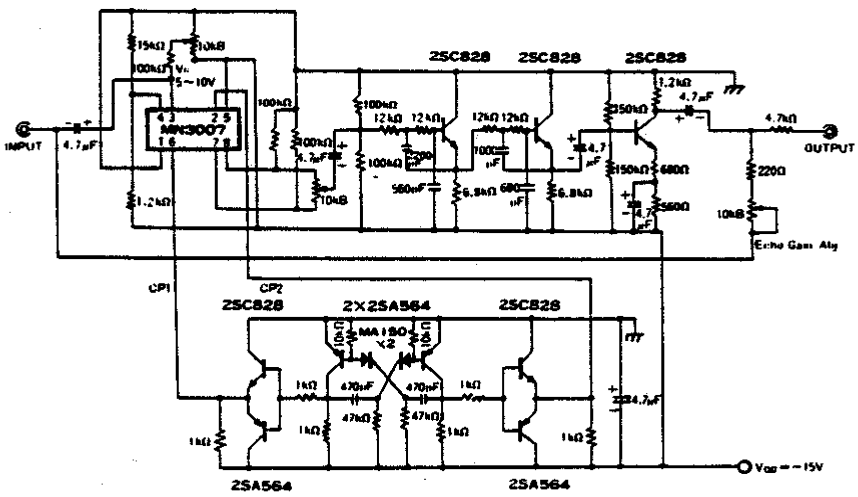








Application Circuit



Echo Effect Generation Circuit (Signal Delay Over 10msec.)